

SEMI MS12-0220

SPECIFICATION FOR SILICON SUBSTRATES USED IN FABRICATION OF MEMS DEVICES

This Standard was technically approved by the MEMS/NEMS Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on December 12, 2019. Available at www.semiviews.org and www.semi.org in February 2020.

1 Purpose

1.1 Although the substrates used in the production of MEMS share many physical and electrical properties with those used in IC manufacturing there are some significant differences as well. There exists a need to standardize MEMS substrates to allow the stocking of standard material, lowering the time to purchase, time to market and overall cost. This specification provides the necessary information for ordering and specifying such substrates.

2 Scope

2.1 This Document can be used as a basic purchasing template between the substrate buyer and seller of 150 and 200 mm nominal diameter substrates.

2.2 This Document contains the information needed to specify selected categories of substrates used in MEMS manufacturing including information on physical properties such as dimensions and surface properties as well as basic electrical properties.

2.3 The values for characteristics, which have been historically agreed upon between supplier and user are listed in tabular form in this Specification. Where values have not been historically agreed upon, the property has been listed with a value to be specified between the buyer and seller.

2.4 One or more methods for measurements used to determine the tabulated characteristics are included where practical.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Specification does not cover all the various forms of the substrates that can be used for MEMS manufacturing nor does it cover all characteristics of such substrates.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D4 — Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

SEMI 3D13 — Guide for Measuring Voids in Bonded Wafer Stacks

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI MF533 — Test Method for Thickness and Thickness Variations of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

4.2 ASQ Standard¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

4.3 ASTM Standard²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, with Specified Precision, the Average for a Characteristic of a Lot or Process

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 BOX — buried oxide

5.1.2 SOI — silicon on insulator

5.2 Definitions

5.2.1 *back surface* — the exposed surface opposite to that upon which devices have been or will be fabricated, typically containing the SEMI M12, SEMI M13, or SEMI T7 marking. In cases where there is no difference between the front and back surfaces, then the surfaces may be determined arbitrarily, and are therefore interchangeable until a SEMI M12, SEMI M13, or SEMI T7 mark has been established.

5.2.2 *bow* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. [SEMI M59]

5.2.3 *constrained condition* — the state of a wafer under test, when one side of the wafer is clamped to an ideally flat surface; for example, when pulled down by a vacuum onto an ideally clean flat chuck.

5.2.4 *device layer* — active layer of prime quality silicon that is typically thinner and used for MEMS device and/or integrated circuit (IC).

5.2.5 *edge exclusion (EE), nominal* — the distance from the FQA boundary to the periphery of a wafer of nominal dimensions. [SEMI M59]

5.2.6 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion, EE, over which the specified values of a parameter apply. Because the nominal edge exclusion relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances. [SEMI M59]

5.2.7 *front surface* — the exposed surface upon which devices have been or will be fabricated, typically the surface opposite to that containing the SEMI M12, SEMI M13, or SEMI T7 marking. In cases where there is no difference between the front and back surfaces, then the surfaces may be determined arbitrarily, and are therefore interchangeable until a SEMI M12, SEMI M13, or SEMI T7 mark has been established.

5.2.8 *handle wafer* — support wafer, bulk silicon or sapphire; may also be referred to as carrier wafer.

5.2.9 *lot* — for the purposes of commercial exchange of wafers, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above that have been identified by the supplier as constituting a lot.

5.2.10 *median surface, of a wafer* — the locus of points equidistant from the front and back surfaces of the wafer. [SEMI HB1]

5.2.11 *reference plane* — a plane from which deviations of a specified surface of the wafer are measured. [SEMI M59]

¹ American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: +1.414.272.8575, Fax: +1.414.272.1734, <http://www.asq.org>

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>