

SEMI MS13-0221

GUIDE FOR USE OF TEST PATTERNS FOR CHARACTERIZING A DEEP REACTIVE ION ETCHING (DRIE) PROCESS

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1 Purpose

1.1 Deep reactive ion etching (DRIE) is widely used in MEMS fabrication processes for creating high-aspect ratio anisotropic features. Further, the etch performance is dependent on open area (OA), that is, the amount of area subject to the etch process, which can range from 1% to 60%. It is also dependent on geometric pattern loading effects, the depth of the etch, the materials to be etched and their preparation. The optimal parameters values chosen vary widely according to the type of MEMS device and application. In addition, each tool type—and often each process chamber—has unique recipe settings for optimum etch performance for each material (typically silicon or silicon dioxide) and pattern. These settings include gas flows, duration, temperature profile, etc. The chamber's environmental conditions also play a role in etch performance and are usually not known to the designer before bringing a design to the foundry. These variables lead to significant costs to both the designer and the foundry, as the process must be tuned to the specific pattern and material combination before production can commence.

2 Scope

2.1 This Document describes a set of etch test structures for characterizing the performance of DRIE process tools.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The results of etching using these test structures are valid only for the DRIE tool used. Other tools, even those nominally identical to the tool used, may give substantially different results.

3.2 These etch test structures are intended for use on 150 mm and 200 mm wafers although other wafer sizes could be considered.

3.3 Use of the test pattern for investigating DRIE on a non-planar surface, for example, with patterning below the material to be etched, may provide different results from a planar surface.

3.4 The results of etching may be dependent on the pattern location and potentially, on the pattern orientation with respect to the crystal plane of the wafer.

3.5 Results may vary according to masking materials and preparation methods used.

3.6 Biasing of mask data may be necessary to achieve consistent dimensions.

3.7 The test pattern is for etch characterization purposes only and does not imply suitability of those dimensions for actual device design.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D5 — Guide for Metrology Techniques to be Used in Measurement of Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 *BOX* — buried oxide layer

5.1.2 *CD* — critical dimension

5.1.3 *DRIE* — deep reactive ion etching

5.1.4 *OA* — open area

5.1.5 *SOI* — silicon-on-insulator

5.2 Definitions

5.2.1 *anisotropic* — exhibiting different physical properties in differing crystallographic directions. [SEMI M59]

5.2.2 *anisotropic etch* — a selective etch used to fabricate micromechanical structures that exhibits an accelerated etch rate along a specific direction. [SEMI M59]

5.2.3 *black silicon* — an imperfectly etched material that may be seen in the larger pad areas, commonly called black silicon or ‘grass’.

5.2.3.1 *Discussion* — The balance between the etch and the passivation deposition phase of the DRIE process means that the respective open areas on the same mask layout can etch very differently. When the process is finally tuned, black silicon or ‘grass’ may be seen in the larger pad areas. This effect is not ideal as this imperfectly etched material can easily break off the substrate and cause catastrophic failure of the devices.

5.2.4 *bottom critical dimension (CD)* — the lateral feature dimension at the bottom of the etched feature.

5.2.5 *buried oxide layer (BOX)* — the silicon dioxide layer between the SOI layer and the base silicon substrate. [SEMI M59]

5.2.6 *deep reactive ion etching* — a time multiplexed process that includes etch and deposition steps that enable fast anisotropic etching of silicon.

5.2.7 *depth uniformity (%)* — the percentage variation in the etch depth across the wafer.

5.2.8 *device asymmetry* — the etch features evaluated for asymmetry, where a side of the feature may have a different angle, scalloping, roughness or depth than its opposite side.

5.2.8.1 *Discussion* — This is typically measured to within 5 mm of the edge of the wafer, although some companies may choose to measure to within 3 mm of the edge of the wafer.

5.2.9 *etch rate* — the total etch depth divided by the total plasma process time, typically given in $\mu\text{m}/\text{min}$.

5.2.10 *etch test structure* — structures that are designed to aid in the characterization of microelectronic and micromachining etch processes. Electrical, optical, or physical measurements can be made on these test structures for the purpose of device evaluation and process optimization.

5.2.11 *mask undercut* — the lateral distance measured under the mask edge to the top of the etched feature.

5.2.12 *open area* — the percentage of the total wafer area that is exposed/available for etching. The area that is not protected by the mask.

5.2.13 *plasma process time* — the total time the plasma is applied (i.e., ignited).

5.2.14 *post-etch feature size* — as measured on the top wafer surface.

5.2.15 *pre-etch feature size* — as defined on wafer in the mask material.

5.2.16 *profile angle ($^{\circ}$)* — the profile angle is typically measured from the horizontal plane of the wafer surface.

5.2.17 *scallop* — a repeated sidewall feature resulting from the gas switching in the deep reactive ion etching (DRIE) process.

5.2.18 *scallop size* — consists of two dimensions: the lateral dimension (from the peak to the trough of the scallop) and the vertical dimension (from one peak of the scallop to the next).

5.2.19 *selectivity to mask* — the mask thickness before and after etching is measured. The amount removed is then compared to the depth of the etch and the resulting ratio is known as the selectivity and is typically denoted by X:1.

5.2.20 *selectivity to oxide* — compares the average silicon etch rate to the calculated respective etch rate for the amount of oxide removed at the end of the etch to give a selectivity.

5.2.21 *sidewall roughness* — the non-repeating irregularities of the sidewall surface texture.

5.2.21.1 *Discussion* — The sidewall roughness is not the same as scallops. Sidewall roughness has various origins. Some relate to the mask, some to the breakdown of the passivation on the sidewall, while others relate to the process conditions. It is typically monitored through scanning electron microscopy (SEM) and the location on the sidewall identified. Sidewall roughness can lead to particles and residues on the wafer's surface.

5.2.22 *SOI layer* — the single crystalline (monocrystalline) silicon film that is separated by an insulating layer, typically but not necessarily silicon dioxide (SiO_2), from a base silicon substrate. Note that polycrystalline or amorphous silicon films on oxidized silicon wafers are not considered to be SOI layers. [SEMI M59]

5.2.23 *SOI wafer* — a multilayer structure of oxide and silicon with a thin film of silicon separated from a base silicon substrate by a buried oxide layer (BOX). [SEMI M59]

5.2.24 *subpattern* — any piece of the test pattern for a specific device function.

5.2.25 *target profile* — a model edge profile constructed by using specified or otherwise pre-selected edge profile parameters.

5.2.26 *test pattern* — the entire design within the exposure area that may be repeated across the wafer.

5.2.27 *tilt* — the non-perpendicular angles of etch, or feature(s) that are intended to be etched straight down, perpendicular to the wafer surface.

5.2.28 *top critical dimension (CD)* — measured below mask undercut where the anisotropic etch process began.

5.2.29 *trench aspect ratio* — the depth of a trench divided by its width.

5.2.29.1 *Discussion* — A trench greater than 15:1 is considered 'high aspect ratio'. Best practice is to measure the width of the etched feature, not the mask that defines the feature.

5.2.30 *undercut, also known as footing, at SOI interface* — the lateral etching of silicon under the oxide interface layer that exceeds the dimensions etched in the oxide layer, thereby undermining the oxide layer.

5.2.31 *wafer size* — typically a measurement of the diameter of the wafer from one edge to the other through the center of the wafer.

6 Test Pattern

6.1 This Guide provides a 22 mm × 22 mm test pattern, consisting of arrays of square, rectangular, and comb finger openings, which can be used as is, or from which elements can be extracted to develop a test pattern for their particular application based on the device functions described in Table 1.

6.2 The OA ranges from 1% to 60% in the test pattern area as described in ¶ 6.1. Each subpattern represents a specific device function, with typical trench aspect ratio and dimensions; for an overview of these see Table 2. It is assumed that the as drawn feature is transmitted onto the mask using the same steps as would be included in the device process, that is, if the process includes compensation structures and or compensation for mask transfer effects, these would also be applied to the etch test structures.

Table 1 Open Area (OA) as Related to Device Function

<i>MEMS Device Function</i>	<i>Opening Type</i>	<i>Open Area Range</i>	<i>Recommended Etch Depth Aspect Ratio (depth-to-width dimension)</i>
Cavity Devices (such as microphone, ultrasound transducer, etc.)	Circle, hexagon, square	10%–60%	0.1:1–1:1
TSV	Circle, square, rectangle	1%–5%	10:1–25:1
Electrostatic (such as inertial sensors, actuators, etc.)	Comb finger	10%–20%	5:1–10:1
Membrane Devices (such as pressure sensors, calorimeter, etc.)	Circle, square	40%–50%	0.5:1–2:1 (through-wafer)
Microfluidics	Slit, rectangle, circle	10%–50%	1:1–10:1
Mirror, Bolometer	Slit, arc	5%–20%	0.5:1–2:1

6.3 General targets for OA are 1% to 5% for hole and slit etch typical of microphone and TSV; 10% to 20% for comb finger etch typical for electrostatic devices such as accelerometers, gyroscopes, actuators, bolometers and mirrors; and 50% for cavity etch for microfluidics, pressure sensor and membrane devices. Detailed dimensions of the features are shown in Table 2. Details of several of the design patterns are shown in Figures 1 through Figures 3. The etch depth should be selected by the user for their application to achieve the aspect ratio shown in Table 1.

6.4 A GDS-II file containing the layout of this pattern is available on the SEMI Standards web site, under Supplementary Materials. Each subpattern is identified by a code from which the opening type, dimensions, spacing, OA, and suggested application can be read from Table 2.

Table 2 Design Dimensions and OA of Etch Test Structure Arrays

2-1 Opening Type: Square							
<i>Code</i>	<i>Opening Type</i>	<i>X (μm)</i>	<i>Y (μm)</i>	<i>Pitch X (μm)</i>	<i>Pitch Y (μm)</i>	<i>OA (%)</i>	<i>Typical Application</i>
A01	Square	5 μm	5 μm	20 μm	20 μm	6.25%	Microphone, TSV
A02	Square	5 μm	5 μm	25 μm	25 μm	4.00%	Microphone, TSV
A03	Square	5 μm	5 μm	35 μm	35 μm	2.00%	Microphone, TSV
A04	Square	5 μm	5 μm	50 μm	50 μm	1.00%	Microphone, TSV
A05	Square	50 μm	50 μm	70 μm	70 μm	51%	Microphone, Microfluidics, Membrane or Cavity
A06	Square	50 μm	50 μm	100 μm	100 μm	25%	Microphone, Microfluidics, Membrane or Cavity
A07	Square	500 μm	500 μm	1000 μm	1000 μm	25%	Microphone, Pressure Sensor, Microfluidics, Membrane or Cavity
2-2 Opening Type: Rectangle							
B01	Rectangle	2 μm	50 μm	12	60	13.89%	Microfluidics
B02	Rectangle	2 μm	50 μm	52	100	1.92%	Microfluidics
B03	Rectangle	10	50	20	60	41.67%	Microfluidics
B04	Rectangle	10	50	60	100	8.33%	Microfluidics
B05	Rectangle	50	500	70	520	68.68%	Microfluidics