

SEMI P28-96 (Reapproved 0707) SPECIFICATION FOR OVERLAY-METROLOGY TEST PATTERNS FOR INTEGRATED-CIRCUIT MANUFACTURE

This standard was technically approved by the global Micropatterning Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on April 25, 2007. It was available at www.semi.org in June 2007. Originally published in 1996.

NOTICE: This Standard or Safety Guideline has an Inactive Status because the conditions to maintain Current Status have not been met. Inactive Standards or Safety Guidelines are available from SEMI and continue to be valid for use.

1 Purpose

1.1 This document defines several standard overlay-metrology patterns that are used by metrology equipment users to evaluate and test micropatterning equipment and processes in integrated circuit (IC) manufacturing. These overlay cells may be placed by optional patterning methods onto substrates during the manufacturing process. Usage of the standard overlay patterns is an attempt to provide consistent industrywide use of automated metrology equipment.

2 Scope

2.1 This specification defines general designs that describe the shape, size, design rules, and placement considerations (where appropriate) of several basic patterns for overlay metrology. These standard test patterns can be used for optical, scanning electron beam, and other types of metrology.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The patterns described in this document represent the first pass at an industrywide commonality for the purpose of compatibility among various types of automated metrology equipment. It is not suggested, however, that these test patterns are a full complement or are optimal for all overlay-metrology applications. This document does not attempt to specify how the patterns are to be imaged or measured on the substrate.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI P6 — Specification for Registration Marks for Photomasks

SEMI P18 — Specification for Overlay Capabilities of Wafer Steppers

SEMI P19 — Specification for Metrology Pattern Cells for Integrated Circuit Manufacture

4.2 ASTM Standard¹

ASTM F127-84 — Definition of Terms Relating to Photomasking Technology for Microelectronics

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Definitions

5.1.1 *centerline* — a reference line that is equidistant from opposite edges of a feature.

5.1.2 *feature* — areas within a single continuous boundary (e.g., an aggregate image) that have any physical property that is distinct from the background area outside the feature (e.g., the simplest element of a test pattern, such as a

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single line or bar). Some physical properties that may distinguish the feature are the refractive index, surface roughness, etc.

5.1.3 *feature dimension* — the dimension of interest; such as, the side of a box, bar width, and/or length.

5.1.4 *overlay (micropatterning)* — a vector quantity defined at every point on the wafer. It is the difference, $\vec{O}$, between the vector position, $\vec{P}_1$, of a substrate geometry, and the vector position of the corresponding point, $\vec{P}_2$, in an overlaying pattern, which may consist of photoresist. [SEMI P18-92]

NOTE 1: All overlay test patterns are designed to provide both X and Y components of the vector overlay.

5.1.5 *pattern, overlay test* — a group of features for overlay metrology.

5.1.6 *pitch* — the distance between a point on an image and the corresponding point on the corresponding image in an adjacent functional pattern.

5.1.7 *substrate (materials)* — in semiconductor technology, a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits. [ASTM F1241-89] NOTE: The meaning of substrate is not limited to wafers.

6 General Specification

6.1 Introduction

6.1.1 This specification describes the overlay test patterns that are illustrated in the figures at the end of this document. The imaging means by which these test patterns are defined on the substrate may be selected by the user (see ¶ 6.2.1).

6.1.2 Characteristics of the overlay patterns, such as materials, topography, polarity, and method of pattern transfer will be defined by the user unless otherwise noted. When reporting measurements extracted from these overlay test patterns, the user should state the physical conditions (e.g., photoresist island on metal over an oxide window). The user should further state which features constitute the substrate geometry and which constitute the overlaying pattern (terms as used in the definition of overlay in ¶ 5.1.4). In general, the vectors P_1 and P_2 terminate at the geometrical centers of the substrate pattern and the overlaying pattern respectively.

6.2 Applications

6.2.1 The overlay test patterns are intended to be used in a variety of applications. The following applications list shows some uses for the overlay test patterns.

- Primary Pattern Generation
- Lithography and Metrology Equipment Characterization
- In-Line Process Overlay Monitoring
- Manufacturing Characterization
- Process Transfer Between Manufacturing Sites

6.3 Guidelines

6.3.1 The overlay test patterns described herein represent a basic metrology set from which composite patterns may be constructed.

6.3.2 Each overlay test pattern has a fundamental design. The user may adjust the dimensions appropriately as they apply to the user's specific processing/equipment situations.

6.3.3 It is required that labels, border lines, indicator marks, or any other adjacent features be avoided, or at least separated by a minimum of ten (10) micrometers from the overlay cell. This proximity guideline is defined to remind the user that patterns intended to be independent and symmetric be designed as circumstances permit. The user should determine actual spacing values, because spacing may be level-, process-, and/or tool-dependent.

6.3.4 It is recognized that there are design limitations dictated by the equipment and processes used to generate the pattern (e.g., computer aided graphics (CAD) grids, pattern generation (PG) rectangles, E-beam spot sizes). The user