SEMI PV22-0321
SPECIFICATION FOR SILICON WAFERS FOR USE IN PHOTOVOLTAIC SOLAR CELLS

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1 Purpose

1.1 This Specification covers the requirements for silicon wafers for use in photovoltaic (PV) solar cell manufacture. To permit common processing equipment to be used in multiple fabrication lines, it is essential for the wafer dimensions to be standardized.

1.2 This Specification provides standardized dimensional and certain other common characteristics of silicon wafers based on currently widely used sizes for photovoltaic applications.

1.3 This Specification also provides a tabular specification format for order entry so that relevant non-standardized wafer characteristics and extensions of wafer sizes for research, development, and new requirements can be easily and consistently specified in commercial transactions.

2 Scope

2.1 This Specification covers ordering information and certain requirements for single crystal silicon wafer and cast silicon wafer for PV applications.

2.2 This Specification allows growth methods that include Czochralski (Cz) method, Floating Zone (FZ) method for single crystal silicon wafers, and casting method with and without seed for cast silicon wafer.

2.3 The specified cast silicon wafer includes cast silicon category I wafer and cast silicon category II wafer.

2.4 A complete purchase specification requires that various physical properties be specified along with test methods suitable for determining their magnitude. The specification format in this Standard provides a comprehensive listing of such properties and available associated test methods (see Appendix 1).

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M44 — Guide to Conversion Factors for Interstitial Oxygen in Silicon

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

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SEMI MF391 — Test Method for Minority Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF533 — Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF978 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1188 — Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

SEMI MF1982 — Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography

SEMI PV1 — Test Method for Measuring Trace Elements in Silicon Feedstock for Silicon Solar Cells by High-Mass Resolution Glow Discharge Mass Spectrometry

SEMI PV9 — Test Method for Excess Charge Carrier Decay in PV Silicon Materials by Non-Contact Measurements of Microwave Reflectance After a Short Illumination Pulse

SEMI PV13 — Test Method for Contactless Excess-Charge-Carrier Recombination Lifetime Measurement in Silicon Wafers, Ingots, and Bricks Using an Eddy-Current Sensor

SEMI PV25 — Test Method for Simultaneously Measuring Oxygen, carbon, Boron and Phosphorus in Solar Silicon Wafers and Feedstock by Secondary Ion Mass Spectrometry

SEMI PV28 — Test Method for Measuring Resistivity or Sheet Resistance with a Single-Sided Noncontact Eddy-Current Gauge

SEMI PV39 — Test Method for In-Line Measurement of Cracks in PV Silicon Wafers by Dark Field Infrared Imaging

SEMI PV40 — Test Method for In-Line Measurement of Saw Marks on PV Silicon Wafers by a Light Sectioning Technique Using Multiple Line Segments

SEMI PV41 — Test Method for In-Line, Noncontact Measurement of Thickness and Thickness Variation of Silicon Wafers for PV Applications Using Capacitive Probes

SEMI PV52 — Test Method for In-Line Characterization of Photovoltaic Silicon Wafers Regarding Grain Size

3.2 *ANSI Standards*[1]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, http://www.ansi.org

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3.3 *ASTM Standard*[2]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for a Characteristic of a Lot or Process

3.4 *EN Standards*[3]

EN 50513 — Solar Wafers – Data Sheet and Product Information for Crystalline Wafers for Solar Cell Manufacturing

3.5 *ISO Standards*[4]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence (TXRF) Spectroscopy

3.6 *JEITA Standards*[5]

JEITA EM-3501 (18) — Standard Methods for Determining the Orientation of a Semiconductive Silicon Single Crystal

3.7 *JIS Standards*[6]

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms and acronyms relating to silicon and other semiconductor technology are defined in SEMIM59.

4.2 *Other Acronyms Used in This Standard*

4.2.1 *μ-PCD* — microwave photoconductance decay

4.2.2 *GDMS* — glow discharge mass spectrometry

4.2.3 *LATF* — local thickness fluctuations

4.2.4 *PV* — photovoltaic

4.2.5 *QSSPC* — quasi steady state photoconductance

4.3 *Other Terms Used in This Standard*

4.3.1 *brick* — one or more squared, cropped, and ground sections from an ingot.

4.3.2 *cast silicon* — crystalline silicon produced by a casting method.

NOTE 1: Wafers cut from cast silicon ingots are typically multicrystalline with grain sizes up to several centimeters, but, depending on the specific casting method used, single crystalline or nearly single crystalline wafer, sometimes called quasi-monocrystalline wafer, may also be obtained.

4.3.3 *ingot* — a cylindrical or rectangular solid of silicon resulting from a crystallization process, generally of slightly irregular dimensions.

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org

[3] European Committee for Standardization, Avenue Marnix 17, B-1000 Brussels; Telephone: +32.2.5.50.08.11, Fax: +32.2.5.50.08.19, http://www.cen.eu

[4] International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56, CH-1211 Geneva 20, Switzerland; Telephone: +41.22.749.01.11, Fax: +41.22.733.34.30, http://www.iso.org

[5] Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

[6] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, http://www.jsa.or.jp

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4.3.4 *monocrystalline* — a body of crystalline material that contains no large-angle boundaries or twin boundaries. (Synonym: *single crystal.*)

4.3.5 *multicrystalline* — a body of crystalline material that contains large-angle boundaries or twin boundaries. Most crystals of this body have dimensions in the millimeter up to centimeter range.

4.3.6 *percentage of the largest single grain* — the area ratio of the largest grain with the same defined crystallographic orientation to the area of the case silicon wafer, expressed in percent.

5 Ordering Information

5.1 Purchase orders for silicon wafers furnished to this Specification shall include the following items. These items are indicated in the Specification Format for Order Entry, Parts 1 and 2, shown in TableA1-1 with a ♦ symbol in the left-most column.

- 2-1.2 Crystallization Method
- 2-1.3 Crystallinity (Single crystal or cast silicon category I, II wafer)
- 2-1.4 Shape (Square or Pseudo-square)
- 2-2.1 Nominal Size
- 2-2.3 Average Thickness
- 2-2.4 Average Thickness Tolerance
- 2-3.1 Conductivity Type
- 2-3.2 Dopant
- 2-3.3 Bulk Resistivity or Sheet Resistance
- 2-3.4 Location of Resistivity Measurement
- 2-3.5 Effective Minority Carrier Lifetime
- 2-4.1 Oxygen Concentration
- 2-4.2 Carbon Concentration
- 2-4.3 Bulk Iron Content
- 2-5.1 Dislocation Etch Pit Density (required for single crystal wafers only)
- 2-5.2 Crystallographic Orientation (required for single crystal wafers only)
- 2-5.3 Edge Orientation (required for single crystal wafers only)
- 2-5.4 The percentage of the largest single grain (required for cast silicon wafers only)
- 2-5.5 Orientation of the largest single grain (required for cast silicon wafers only)

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures (see ¶ 7.2),

5.3.2 Certification (if required) (see § 9),

5.3.3 Packing and marking (see § 10),

5.4 *Optional Criteria* — Any of the remainder of the items listed in Table A1-1 may be specified optionally in addition to those listed above:

5.5 In all cases, it is essential that all choices for the items included in the purchase order be made in order not to have undefined parameters that would lead to surprises between supplier and customer.

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6 Requirements

6.1 *General Characteristics*

6.1.1 The crystallization method shall be as specified on the purchase order.

6.1.2 The crystallinity of the wafer shall be specified as either single crystal or cast silicon category I, II wafer.

6.1.3 The shape of the finished wafer shall be specified as square or pseudo-square.

6.2 *Dimensions and Permissible Variations*

6.2.1 *Wafer Thickness and Thickness Variation*

6.2.1.1 The center point wafer thickness shall be specified.

6.2.1.2 The variation of center point thickness of wafers in a lot shall be less than 5% (or other specified fraction) of the specified wafer thickness.

6.2.1.3 The total thickness variation within a wafer shall be specified.

6.2.2 *Square Wafer Dimensions*

6.2.2.1 Square wafers have straight chamfers at the corners. The typical chamfer angle α, between the wafer edge and the straight chamfer is 45°, but there is no specification for this angle.

6.2.2.2 The allowable dimensions of square wafers are indicated in Figure 1 and Table 1.

6.2.2.3 The specified dimensions are the wafer edge lengths, A, the diagonal, G (to insure squareness of the wafer edges), and the chamfer width, H. All dimensions are given in millimeters. Other dimensions in Figure 1 can be calculated from the specified dimensions using ordinary trigonometric functions.

6.2.2.4 Dimension H is specified to be identical for all sizes, but by agreement between supplier and customer, one of the four corner chamfers can be of different size to indicate the orientation of the wafer.

6.2.2.5 *TTV* — For all wafer sizes, the maximum TTV shall not exceed 30 µm (or other specified amount).

6.2.2.6 *Warp* — For all sizes of square wafers, the maximum warp shall not exceed 75 µm (or other specified amount).

NOTE 2: The areas of square wafers are given for information in Related Information 1.

6.2.3 *Pseudo-Square Single Crystal Wafer Dimensions*

6.2.3.1 Pseudo-square wafers are cut from a circular single-crystal boule and have round chamfers at the corners.

6.2.3.2 The allowable dimensions of pseudo-square single crystal wafers are indicated in Figure 2 and Table 2. These wafers have rounded chamfers of equal size on all four corners.

6.2.3.3 The specified dimensions are the wafer edge length, A, the diameter, D, and the chamfer distance, F, which is the length of a leg of a right isosceles triangle. Because F is the same for all corners, the center of the square of dimension A is the same as the center of the circle of diameter D. All dimensions are given in millimeters. The dimension, C, also shown in Figure 2 can be calculated as the length $A - 2F$.

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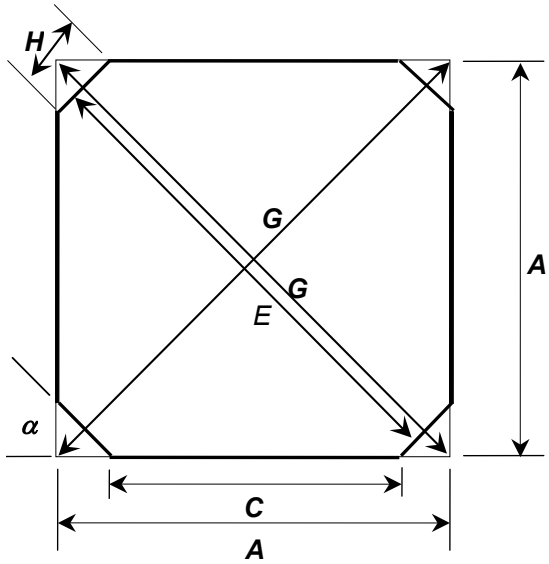

Figure 1
Dimensions of Square Single Crystal Silicon Wafers for PV Solar Cell Applications

Table 1 Dimensions of Square Silicon Wafers for PV Solar Cell Applications

Symbol in Figure 1[#1]		*Dimensions*		
Dimension Name		*A (mm)* *Wafer Edge Length*	*G (mm)* *Diagonal*	*H (mm)* *Chamfer Length*
Nominal Size (mm)	100.75	100.75 ± 0.25	142.4 ± 0.5	1.25 ± 0.75
	125.75	125.75 ± 0.25	177.8 ± 0.5	1.25 ± 0.75
	156.75	156.75 ± 0.25	221.6 ± 0.5	1.25 ± 0.75
	158.75	158.75 ± 0.25	224.5 ± 0.5	1.25 ± 0.75
	166	166 ± 0.25	234.76 ± 0.5	1.25 ± 0.75
	210	210 ± 0.25	296.98 ± 0.5	2 ± 0.65
Symbol in EN 50513		A, B	C	D
Symbol in SEMI M6		A, B	C	D

#1 The letter symbols in Figure1 differ as indicated from those in both the previous SEMI Specification for silicon wafers for solar cell application (SEMI M6, now superseded by this Standard), and EN 50513. Note that both SEMI M6 and EN 50513 used a different symbol for each of the two wafer edge lengths. The dimensions shown in Figure 1 by C, E, and α do not appear in SEMI M6. The dimension E is taken from EN 50513, but values are not specified here because they are determined from the combination of G, and H.

6.2.3.4 *TTV* — For all sizes of pseudo-square wafers, the maximum TTV shall not exceed 30 µm (or other specified amount).

6.2.3.5 *Warp* — For all sizes of pseudo-square wafers, the maximum warp shall not exceed 75 µm (or other specified amount).

NOTE 3: The areas of pseudo-square wafers are given for information in Related Information1.

6.3 *Materials and Manufacture*

6.3.1 The material shall consist of wafers conforming to the crystallinity class specified in the purchase order or contract.

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