

SEMI PV41-0912 (Reapproved 0419) TEST METHOD FOR IN-LINE, NONCONTACT MEASUREMENT OF THICKNESS AND THICKNESS VARIATION OF SILICON WAFERS FOR PHOTOVOLTAIC APPLICATIONS USING CAPACITIVE PROBES

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1 Purpose

- 1.1 Wafer thickness and its variation across a wafer are important parameters for solar cell manufacturing. Excessive thickness variations within a lot from wafer to wafer or within a wafer may negatively impact process yield and solar cell efficiency.
- 1.2 Both parameters are part of the specification for solar cell wafers (SEMI PV22), which define a thickness range as well as an upper limit for the total thickness variation (TTV).
- 1.3 In addition, careful process and quality control of the wafer thickness and its variation during wafer and solar cell manufacturing requires continuous monitoring of thickness by the supplier of wafers for photovoltaic (PV) applications as well as by the user of such wafers.
- 1.4 Therefore a standardized test method providing reproducible data for thickness and its variation is required to establish agreement between business partners regarding the specification of wafers.
- 1.5 The present Document defines a noncontact, high throughput in-line method for measuring wafer thickness and its total variation using capacitive probes.

2 Scope

- 2.1 This Test Method covers the in-line, noncontact, nondestructive measurement of the thickness and the TTV of clean, dry silicon (Si) wafers supported on two belts that move the test specimen through the measurement equipment.
- 2.2 The test method is applicable to square or pseudo-square multi- as well as single-crystalline Si wafers in the resistivity range $10^{-3} \Omega \cdot \text{cm}$ to $10^5 \Omega \cdot \text{cm}$ with edge length $\geq 125 \text{ mm}$ and with thickness $\geq 100 \mu\text{m}$.
- 2.3 The Test Method is based on simultaneously measuring the capacitance between an aligned pair of capacitive probes and the wafer surfaces when the wafer passes through the gap formed between the capacitive probe pair.
- 2.4 The Test Method does not cover measurement of surface flatness, warp, bow or sori of wafers.
- 2.5 The Test Method is intended for in-line high throughput measurements. Therefore it is mandatory to operate system under tight statistical process control (SPC), for example ISO 11462, in order to obtain reliable, repeatable and reproducible measurement data.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

- 3.1 The Test Method averages the thickness measurement over the size of the active area of the capacitive probes used. Using different sensor sizes therefore may result in different thickness measurement results.
- 3.2 The Test Method averages the thickness measurement over a wafer in constant motion so that areal averaging effects may impact measurement results due to belt speed and triggering differences.
- 3.3 Differences between surface finishes or contamination of the wafers also may affect the measurement results.
- 3.4 Strong variations of the charge carrier concentration within a wafer may impact the measurement result in comparison with other methods for thickness measurement or with differing mechanical and electrical set-ups of capacitive probes.

3.5 Capacitive probes have only a limited calibrated range for distance or thickness measurement. Exceeding this range may result in erroneous measurement results.

3.6 Exceeding the temperature range and humidity range for which the measurement equipment is qualified may also result in erroneous measurement results.

3.7 Different alignments of capacitance probe pairs, such as gap distance, probe centering and probe parallelism, is known to impact thickness measurement results.

3.8 Variations in the positions of the scan lines between subsequent measurements or between measurements on different equipment may impact the measurement results.

4 Referenced Standards and Document

4.1 SEMI Standards and Safety Guidelines

SEMI E89 — Guide for Measurement System Analysis (MSA)

SEMI M59 — Terminology for Silicon Technology

SEMI MF1569 — Guide for Generation of Consensus Reference Materials for Semiconductor Technology

SEMI PV22 — Specification for Silicon Wafers for Use as Photovoltaic Solar Cells

4.2 ISO Standards¹

ISO 11462-1 — Guidelines for Implementation of Statistical Process Control (SPC) – Part 1: Elements of SPC

ISO 11462-2 — Guidelines for Implementation of Statistical Process Control (SPC) – Part 2: Catalogue of Tools and Techniques

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

NOTE 1: Refer to the SEMI International Standards: Compilation of Terms (COTs) for a list of the most current terms and their definitions.

5.1 Terms and acronyms relating to silicon and other semiconductor technology are defined in SEMI M59.

5.2 Other Abbreviations and Acronyms

5.2.1 *MSA* — measurement system analysis

5.3 Other Terms Used in this Standard

5.3.1 *active area, of capacitive probe* — the area of the capacitive probe over which the signal is collected.

5.3.2 *capacitive probe* — a probe with an exposed planar metal surface area (the active area) that acts as one plate of a capacitor. It is used to measure the capacitance between the probe and a surface of a conducting or semiconducting object, which acts as the other plate of a capacitor. The distance from the probe to the other planar surface can be calculated if within a calibrated range.

5.3.3 *center line (CL)* — an imaginary straight line bisecting a square or pseudo-square wafer surface. It is equidistant from opposing edges of the wafer surface.

5.3.4 *guard ring, of capacitive probe* — a metal ring around the active area of a capacitive probe and electrically separated from it, screening the active area from stray fields.

5.3.5 *three line scan (L3)* — the thickness data acquisition technique using three pairs of stationary capacitive probes and a wafer transport belt system. The three scan lines consist of the center scan line, and two outer scan lines on opposite sides of it and offset equidistantly towards the wafer edges.

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5.3.6 *offset distance (OD)* — the distance between the trigger point where the measurement is started or terminated and the point where the first or last data, respectively, are recorded.

5.3.7 *scan line (SL)* — an imaginary line parallel to a wafer edge and parallel to the wafer transport direction along which measurements are performed. Several scan lines per wafer may be used.

5.3.7.1 *center scan line* — a scan line nominally aligned to the center line of the wafer.

5.3.7.2 *outer scan line* — a scan line, parallel to the center scan line and removed from it toward a wafer edge.

5.3.8 *thickness, average (L3TA)* — an arithmetic average over all thickness values measured by the three probe pairs by a three line scan of a wafer between the trigger points plus-minus the offset distances.

5.3.9 *thickness, 5-point (L3T5)* — the average over the thickness measured at five points on the wafer by a three line scan. Four points are located after or before the trigger points, respectively, on the outer scan lines by the offset distance *OD*. The fifth point is the center point on the center scan line.

5.3.10 *thickness, 9-point (L3T9)* — the average over the thickness measured at nine points on the wafer by a three line scan. Three points each are from the center scan line and the two outer scan lines. Along each scan line the three points are located at the trigger points plus-minus the offset distances and at the midpoint. An example is *L3T9*.

5.3.11 *thickness, center point (L3TC)* — the thickness at the midpoint of the center scan line.

5.3.12 *total thickness variation (L3VA)* — the measurement range or difference between the maximum and minimum of all the thickness values used to calculate the average thickness *L3TA*.

5.3.13 *total thickness variation, 5-point (L3V5)* — the measurement range or difference between the maximum and minimum of the thickness values used to calculate the 5-point average thickness *L3T5*.

5.3.14 *total thickness variation, 9-point (L3V9)* — the measurement range or difference between the maximum and minimum of the thickness values used to calculate the 9-point average thickness *L3T9*.

5.3.15 *trigger point* — the point along a scan line where the measurement is started or stopped, respectively. There are two trigger points per scan line, the start trigger point where the measurement is started and the stop trigger point where the measurement is stopped.

6 Summary of Test Method

6.1 The wafer resting on two belts is moved by the belts between three aligned pairs of opposing capacitive probes. The pairs of probes are named *A*, *B* and *C* (see Figure 1).

6.2 The wafer is oriented so that the saw marks are perpendicular to the transport direction of the belts, and the centerline of the wafer intersects the center of the middle probe-pair, *B*.

6.3 The scan lines of the *L3* data acquisition are therefore named *SL a*, *SL b* and *SL c*, where *SL b* is along the *CL*.

6.4 Consecutive measurements of the sum of the distances between the capacitive probes of a pair and the nearest wafer surfaces are performed along the center scan line *SL b*, and the outer scan lines *SL a* and *SL c* (Figure 1) as the wafer is moved along by the belts between the capacitive probes. A pair of measured capacitance values can be used to determine the distances of the front surface to the upper capacitance probe and the back surface to the lower capacitance probe.

6.5 The wafer thickness is then the sum of the measured distance pair and the known distance between the pair of aligned probes.

6.5.1 The known distance between the pair of aligned probes is well established using thickness calibration procedures, typically with traceable thickness reference materials.

6.6 The wafer data acquisition is started and stopped by a pair of trigger sensors located close to each of the capacitive probes so that within-wafer measurement positions may be calculated independent of wafer arrival timing based on trigger timing, the time base and the known belt speed.

6.7 Wafer thickness as a function of position is recorded along each scan line between the start and stop trigger points.

6.8 Metrics of thickness and thickness variation are then reported per wafer.

7 Interferences

7.1 *Contamination* — In the space between the probes as well as on the wafer or probe surfaces may impact the measurement result.

7.2 *Misalignment* — Within a pair of probes may also impact the measurement result.

8 Apparatus

8.1 *Capacitive Probes* — Three pairs of opposing capacitive probes are aligned in a row perpendicular to the belt direction and mounted so that a wafer on the belts traverses midway between the probes of each pair (see Figures 1 and 2).

8.1.1 The distance between the probe surfaces of a pair is $w \pm \Delta w$, with the tolerance Δw according to the specifications of the supplier of the capacitive probes.

8.1.2 The outer probes (*A* and *C*) have a circular active area with a diameter of d_1 or a rectangular area with the size of d_2 by d_3 .

8.1.3 The middle probe *B* has a rectangular active area with a size of d_2 by d_3 or a circular active area with a diameter d_1 .

8.1.4 The outer probe centers are equidistant from the center line and are set at a distance l_2 from the wafer edges where that l_2 is in the range of 8 mm to 15 mm.

8.1.5 The center-to-center distance of middle probe to outer probes on each side is l_1 and depends on wafer size in order to achieve l_2 within the range specified above.

8.2 *Trigger Sensors* — Pairs of opposing light emitting devices and sensors form light beams that detects the presence of a wafer to start and stop the measurement.

8.2.1 The diameter of the light sensors is d_4 . A pair of trigger sensors is positioned beside each capacitive sensor probe pair along lines parallel to the direction of the wafer movement (see Figure 1), so that the measurement starts or stops, respectively, at a distance $l_3 + e$ from the leading and trailing wafer edges, respectively (see Figure 3).

8.2.2 l_3 has to be $\geq d_1/2$ or $d_2/2$, whatever is larger. The centers of both trigger sensors for probe *A* as well as for probe *C* are off-set from the probe centers, respectively, by $l_3 - d_4/2$ towards the adjacent outer edge and towards the leading and trailing edges of the wafer.

8.2.3 The centers of the trigger sensors for probe *B* are off-set from the probe center by $l_3 - d_4/2$ towards the leading and trailing edges and towards the outer edges of the wafer so that they are opposing each other diagonally.

8.2.4 If the sensors are triggered by a wafer chamfer edge (e.g., for a pseudo square wafer), then:

$$e = (l_3 - \frac{d_4}{2})(1 + \tan \alpha) + \frac{d_4}{2 \cos \alpha} \quad (1)$$

with the chamfer angle α . In all other cases $e = 0$.

8.3 *Electronics* — Controlled by a computer that is equipped with software for recording and processing the measured data according to § 14. Other components, which may be included in the computer, consist typically of a pre-amplifier, de-modulator and a HF generator that drives the probes.

8.4 *Wafer Transport Device* — Consisting of two belts, which transport the wafer continuously through the measurement apparatus and do not obstruct the space between the capacitive probes and the wafer surfaces.

9 Safety Precautions

9.1 The entire equipment has to be placed in a closed housing and has to be secured with a safety lock that stops the belts and safely switches the tool off when the housing is opened.

10 Test Specimen

10.1 Clean, dry Si wafers.

11 Preparation of Apparatus

11.1 The suitability of the equipment is determined by performing a statistically based MSA to ascertain whether the equipment is operating within the manufacture's stated specification (e.g., according to SEMI E89).

11.2 Adjust the position of capacitive probes with respect to the transport belts so that the wafers are placed in the gap between the capacitive probes.

11.3 Verify that the capacitive probes are aligned and adjusted according to the manufacturer's specifications.

11.4 Verify that the equipment is operating within its specified temperature range.

11.5 Define the control limits for SPC for the measurement equipment with a set of selected wafers (see ISO 11462).

11.6 As this Test Method is intended for a high throughput, high volume measurement the equipment cannot be calibrated for measuring each individual wafer. Therefore careful SPC has to be performed.

12 Calibration and Standardization

12.1 The equipment is calibrated by using reference wafers the thickness of which is known at marked positions corresponding to the positions of the capacitive probe pairs and the resistivity of which is in the range $10^{-3} \Omega \cdot \text{cm}$ to $10^5 \Omega \cdot \text{cm}$.

12.2 For calibrating the equipment a reference wafer is positioned in the equipment so that the marked positions are precisely located between the probe pairs *A*, *B* and *C* and that the wafer is in the linear range of the gap of the probe pair.

12.3 For test specimens with a resistivity of $\geq 1 \text{ k}\Omega \cdot \text{cm}$ the electrical resistivity of the reference wafer and the test specimens have to agree within $\pm r\%$. The value of *r* has to be provided by the equipment supplier so that the bias of the thickness measurement is less than 5% of the specified thickness tolerance of the test specimen.

NOTE 2: Such a value for *r* corresponds to a *P/T* ratio of 30%, 6 σ (see SEMI E89).

12.4 The calibration is performed while the transport belts are not moving.

12.5 Calibration is established only for the specified linear range of the capacitive probe pairs about the gap position used during this calibration.

12.5.1 Large changes in product-specified wafer thickness may require changing the calibration when the thickness is changed.

NOTE 3: Thin wafers supported by two belts may display gravitational sag that places the measured parts of the wafer out of the calibrated range between the capacitive probes.

12.5.2 Calibration has to be performed under the same ambient conditions (temperature, humidity, illumination) as the measurements of the test specimens and within the ranges specified by the supplier of the probes.

12.6 Care has to be taken when a tool is selected for establishing the wafer thickness at the reference positions of the reference wafer. This tool shall be calibrated with traceable reference materials and its measurement principle shall correspond to the capacitive probes that are calibrated, in particular regarding their size and dimensions of the active area of the capacitive probes.

13 Procedure

13.1 Adjust the equipment and calibrate it according to the instructions of the supplier.

13.2 Verify the equipment is within the SPC limits.

13.3 Put a wafer on the transport belts.

13.4 Verify that the wafer is positioned within the calibrated range of the probe pairs, as provided by their manufacturer.

13.5 Align the wafer so that two of its edges are parallel to, and the saw marks are oriented perpendicular to, the direction of transport, and that the center line of the wafer coincides with the center of probe *B*.

13.6 Ensure that the tilt of the wafer surface with respect to the probe surface is less than 0.5° .