

SEMI PV48-0613 (Reapproved 0419) SPECIFICATION FOR ORIENTATION FIDUCIAL MARKS FOR PHOTOVOLTAIC SILICON WAFERS

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1 Purpose

- 1.1 Dimensional metrics as described in several SEMI Test Methods do not define wafer physical orientation during measurement.
- 1.2 Measurements of the same wafer differently oriented (rotated or flipped between measurements) result in permuted data sets, within the limits of the measurement equipment precision. This may generate confusion or at least discussions during claim handling or specification verification.
- 1.3 It may also benefit some solar cell process steps to orient a wafer in a specified or preferred orientation.
- 1.4 Therefore orientation fiducial marks are required that allow unique orientation of square or pseudo-square silicon (Si) wafers during measurement or processing.
- 1.5 Many photovoltaic (PV) Si wafers are currently marked to enable tracing and to tracking. These marks may be used also as orientation fiducial marks.
- 1.6 This Specification defines how current marks may be used as orientation fiducial marks.
- 1.7 It defines also how to apply an orientation fiducial mark on an otherwise unmarked wafer.

2 Scope

- 2.1 This Specification covers square and pseudo-square Si wafers for PV applications, with a nominal edge length ≥ 125 mm and a nominal thickness ≥ 100 μm .
- 2.2 It may be applied to single crystalline as well as to multicrystalline Si wafers.
- 2.3 It applies to PV Si wafers that are marked with one of the marks as described in SEMI PV29 and SEMI PV32.
- 2.4 It applies also to wafers with only a fiducial mark according to § 7.2.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

- 3.1 None.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI PV29 — Specification for Front Surface Marking of Photovoltaic Silicon Wafers with Two-Dimensional Matrix Symbols

SEMI PV32 — Specification for Marking of Photovoltaic Silicon Brick Face and Photovoltaic Wafer Edge

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

- 5.1.1 BSC — brick slice code

6 Ordering Information

6.1 *Checklist* — Purchase orders for silicon wafers furnished to this Specification shall include the following items:

- For wafers with ID marks
 - Type of mark used, SEMI PV29 or SEMI PV32.
 - Number and relative orientation of marks.
- For wafers without ID mark
 - Statement if a single notch according to § 7.2 shall be applied or not.

7 Requirements

7.1 *Wafers with ID Marks*

7.1.1 According to SEMI PV29 or SEMI PV32 wafers may have an ID marking for being able to trace them back to their position in the ingot during crystallization and for tracking them through the solar cell manufacturing process.

7.1.2 These ID marks may serve as orientation fiducial marks (see Figure 1):

7.1.2.1 Wafers with front side marks according to SEMI PV29:

7.1.2.1.1 The wafer sides parallel to the finder patterns of the code are defined as a_1 and a_4 when viewing the wafer from above the surface containing the marks.

7.1.2.1.2 The corner of the wafer where a_1 and a_4 meet is defined as K_1 .

7.1.2.2 Wafers with brick slice coding according to SEMI PV32:

7.1.2.2.1 The wafer edge containing the mark is defined as side a_1 according to Figure 3 and the corner K_1 corresponds to the corner closest to the brick ID of this mark.

7.1.2.2.2 If a wafer has two adjacent edges with ID marks then K_1 is the corner where the sides with the marks meet and side a_1 is defined as that side where the brick ID is closest to the corner.

7.1.2.2.3 Brick slice codes on opposing edges of a wafer are not recommended, according to SEMI PV32.

7.2 *Wafers Without ID Marks*

7.2.1 Such wafers will be marked with a single notch on an edge, which could be applied already on the brick (see Figure 2).

7.2.2 The wafer edge containing the notch is defined as side a_1 .

7.2.3 The center of the notch is placed at a distance of $A_1/4 \pm$ notch width from wafer corner K_1 .

7.2.4 The depth and width of the notch are according to SEMI PV32.

7.2.5 The wafer is viewed from the top when the notch is to the right of K_1 .