SEMI T19-1109
SPECIFICATION FOR DEVICE MARKING

This standard was technically approved by the global Traceability Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on September 4, 2009. It was available at www.semi.org in October 2009 and on CD-ROM in November 2009. Originally published July 2008.

1 Purpose

1.1 The purpose of this document is to establish a standard specification of marking on semiconductor devices to identify individual device by unique identification code and possible optional information to suggest a part of manufacturing information.

2 Scope

2.1 The specification document ranges from bare semiconductor dice to be packaged or assembled devices.

2.2 While the document specifies physical interface of marking depending on one or more available technologies, it doesn't restrict specific means of writing, reading alignment and so on.

2.3 The document also handles a part of logical interface about the information of the marking.

2.4 This document does not specify specific means to mark (writing) nor to identify (reading) the mark but guide possible ones implicitly with geometric requirements.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Depending on types of semiconductor devices including their structure and manufacturing process, a part or whole of this specification may not be effective. Users of this standard are required to take care of this specification before producing or during designing process.

3.2 This standard doesn't recommend to put a marking on all device products. It is believed that the marking is expected to such device products that have good balance among device price, writing/reading costs including tools, degree of necessity and so on.

3.3 Because this specification is prepared based on semiconductor devices, the other devices are out of the scope of this standard. However, it could be applied to such devices if implementing the description of this document doesn't hinder property of the devices at least physically. Users of this standard for such devices are responsible for all of the implementation and application of this specification.

4 Referenced Standards and Documents

4.1 *SEMI Standards*

SEMI T13 — Specification for Device Tracking: Concepts, Behavior and Services

SEMI T14 — Specification for Micro ID on 300 mm Silicon Wafers

4.2 *ISO/IEC Standard*[1]

ISO/IEC 16022 — International Symbology Specification – Data Matrix

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

1 International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30; http://www.iso.ch

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5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *DDM* — Die Device Mark

5.1.2 *DM* — Device Mark

5.1.3 *PDM* — Packaged or sealed Device Mark

5.1.4 *SIP* — System In Package; Refer to SEMI Compilation of Terms (COT).

5.2 *Definitions*

5.2.1 *Alignment Bar, of data matrix code symbol* — a solid line of contiguous filled cells abutting a line of alternately filled and empty cells. [ISO/IEC 16022]

5.2.2 *Binary Value* — a value to evaluate a cell of data matrix code symbol. A dot in the data matrix code symbol indicates the binary value 1. The absence of a dot indicates the binary value 0.

5.2.3 *Border Column* — the outermost column data matrix code symbol. This column is a portion of the finder pattern.

5.2.4 *Border Row* — the outermost row of data matrix code symbol. This row is a portion of the finder pattern.

5.2.5 *Cell, of* data matrix *code symbol* — the area within which a dot may be placed to indicate a binary value.

5.2.6 *Complex Device* — a device which consists of more than one subcomponent device. They may be piggy backed, stacked, flipped over, soloed on additional substrate and so on. They may or may not be interconnected. SIP and Hybrid IC devices are a part of examples.

5.2.7 *Data Matrix Code Symbol* — a two-dimensional array of square cells arranged in contiguous rows and columns. In certain ECC200 symbols, data regions are separated by alignment patterns. The data region is surrounded by a finder pattern. [ISO/IEC 16022]

5.2.8 *Device Mark* — marking placed on the surface of semiconductor device to identify the individual device. This is the general term of such mark as Die Mark and Packaged or Sealed Device Mark.

5.2.9 *Die Mark* — marking placed on the surface of semiconductor die to identify the individual die; more formally Die Device Mark.

5.2.10 *Dot, in a cell of data matrix code symbol* — a physical difference to evaluate the value of a cell of data matrix code symbol. The physical difference may be protrusion, hollow, material/density/phase difference and so on, depending on technology of marking.

5.2.11 *Finder Pattern, of data matrix code symbol* — a perimeter to the data region. Two adjacent sides contain dots in every cell; these are used primarily to define physical size, orientation and symbol distortion. The two opposite sides are made up of cells containing dots in alternate cells. [ISO/IEC 16022]

5.2.12 *Hybrid IC* — words listed in SEMI Compilation of Terms (COT). Refer to the SEMI COT.

5.2.13 *Identification, contained in data matrix code symbol* — a code to identify an individual device uniquely with manufacture's assigned code in the same model of products or pointer to external data for such specific purpose as verification.

5.2.14 *Packaged or Sealed Device Mark* — marking placed on the surface of packaged or sealed semiconductor device to identify the individual device; i.e., often the individual die in the package.

6 Fundamental Requirements

6.1 *Space and Margin* — This document assumes that the target device has enough space to place Device Mark and required margins to write, read and align the mark.

6.2 *Unique Identification* — Users of this standard have to take care of identification represented by device mark on each unit of product semiconductor device so that it has unique identification for the purpose of traceability of the device.

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6.2.1 *Relation with Identification on Traceability System* — The identification included in the Device Mark have to be basically equivalent to one managed on united and linked traceability system for the device; refer to SEMI T13.

6.2.1.1 However, sometimes for some devices it may be difficult to be inevitably complete because of difference of the length of the identification between one included in the physical mark and logical one on the system, legacy commercial practice related to the format of the identification, circumstance of device users' industries and so on.

6.2.1.1.1 They shall be identifiable uniquely without any confusion at least in a limited range: e.g., supplier, user, user industry, application, device type, specific assembly/packaging and so no.

6.2.1.1.2 These identifications shall be one-to-one translatable to ones on the system with cluing information which suggests the reduced letters, expected range and/or reason. Direct or indirect users of the devices can claim the information.

7 Overview

7.1 *Manufacturing Semiconductor Devices* — Semiconductor devices are manufactured though processing on the surface of such semiconductor wafer substrate many times. They are diced and assembled with packaging or sealing after the wafer processes. Marking is expected during these process steps.

7.2 *Marking on Semiconductor Devices* — This document specifies marking on dice before making them separated into individual devices. This document also specifies marking on assembled devices during or just after packaging or sealing. This standard requires both of them.

7.3 *Identifying Device Marks in Downstream Manufacturing Processes* — The mark on dice, that is DDM, may be read in downstream semiconductor manufacturing processes and its information may be used to identify individual die or interpreted as a part of process data or parameters of one of such process stages as assembling in a subcontract manufacturer. Also the mark on packaged or sealed devices, that is PDM, may be identified and made use of its information as a part of process information for such process as mounting on Print Circuit Boards (PCB). This standard doesn't require to do that or doesn't restrict to do that because this document is prepared just for traceability. This document state that they could be effective depending on many related conditions; sometimes it's redundant or cost-ineffective, and traceability [information technology] system may provide richer information.

7.4 *Anticipated Capability and Reasonable Cost Corresponding to Required Surface Area and Facility* — To maximize competing area for semiconductor manufacturers and facility suppliers including marking/reading tools and units, this standard specifies more than one possible sets of sub-specification in appendix sections of this document. It also contributes to apply wide variety of semiconductor devices.

8 Requirements

8.1 *Marking on Dice* — A semiconductor die device has a couple of surfaces to mark on. This standard requires to mark on the both of them basically with the same information.

8.2 *Marking on the Fabricating Surface of Bare Semiconductor Device Die* — There are many amount of active and passive elements, and fields to separate, isolate physically or prevent parasitic electric effects and make leading or sealing.

8.2.1 *Position of Marking* — Because there are so many fields and elements as introduced above and making less restriction for designing semiconductor devices especially laying out of elements, electrodes and so on, this standard doesn't specify fixed position of Die Mark on them.

8.2.2 *Buffer Area* — Not to break nor interfere such elements for mark-writers, this specification takes care of buffer area between DDM and them. This includes such consisting factors as repetition positioning accuracy of stage of semiconductor substrate and alignment accuracy of image processing unit of the writers. The area helps mark-readers discriminating between the mark and the field of such elements. This document specifies the integrated area of such factors in distance.

8.2.3 *Depth of Marking* — While a semiconductor device has many fabrication layers, some of them may not have enough thickness to write the mark depending on technology of writing. Even if not, sometimes it may be available for marking when the layer or electrode is independent to the other part electrically or physically. This document just specifies maximum depth that makes change the surface of the layer to be written for the mark. If covering layer(s) are transparent or mark-writing energy is focused just on the surface of the target layer, this document

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specifies the affected depth on the layer by marking. This document doesn't define whether it is just underneath of the surface or reaches to a part of covering layer(s). This standard requires that the marking doesn't make any serious dysfunction or shifting property.

8.3 *Marking on the Rear Surface of Bare Semiconductor Device Die* — Bottom side of bare semiconductor devices have usually no or far less such things as elements and electrodes that abstain Die Marking on the surface. It's almost free to place the mark there. However, it has usually no target mark and no standard way to identify vertexes on the face. This document takes the same manner as the mark on top side of semiconductor devices. Therefore this standard doesn't define such things as specific position of the mark but specifies things like minimum buffer area and so on.

8.4 *Marking on Packaged or Assembled Devices* — Packaged/Assembled devices have less restrictions as rear surface of device dice. Packaged devices are more flexible as they have many possible faces to mark on, for example. With such facts this document specifies limited items like specification of marking on dice as above.

8.4.1 *Surface Condition* — However, semiconductor or electronics industry has various materials and technologies of packaging or sealing of semiconductor devices. Sometimes roughness of their surface may make difficult to write or read mark, or make problem in readability and correctness. Users of this standard are expected to choose better size and appropriate position on the surface.

8.4.2 *Marking Face* — This standard doesn't define specific face to write mark on packaged/assembled devices: i.e., PDM. The party to write the mark has the responsibility to choose the right face and position to maximize the benefit of PDM and avoid misreading or misidentifying.

8.5 *Attributes of Mark* — This standard specifies minimum number of items about device marks in this document. Writing manufacturers on upstream processes shall disclose minimum or sensible information to identify the mark. The information is referred to as attributes here. Associated information such as visual identification target mark may also be included as a part of the attributes. Refer to the Related Information section of this document for example sets of the attributes.

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APPENDIX 1
REQUIREMENTS OF DIE DEVICE MARK (DDM) FOR 100 MICROMETER-TYPICAL DOT MATRIX CODE

NOTICE: The material in this appendix is an official part of SEMI T19 and was approved by full letter ballot procedures on May 13, 2008.

A1-1 One of Specific Device Mark on Semiconductor Device Dice

A1-1.1 *Purpose of this Appendix* — This appendix specifies one of recommended device marks on semiconductor device dice here.

A1-1.1.1 *Expected Technology to Write Mark on Dice* — This appendix doesn't specify or restrict writing process and technologies, writer device type or corresponding reader device units. Any means are possible to use as long as they meet things specified in this appendix and related part of whole this document.

A1-2 Geometric Requirements

A1-2.1 *Type of Mark* — The mark specified here shall be a data matrix code symbol which is composed an array of 20 rows and 20 columns defined in ISO/IEC ISS 16022; refer to Figure A1-1.

A1-2.1.1 *Cells* — Typical cell spacing of data matrix code symbol shall be 5.00 µm. This appendix allows it through 2.50 µm as minimum to 10.00 µm as maximum inclusive, depending on marking technology and occupying cost on semiconductor device dice; refer to left half of Figure A1-2. Surface area of each cell is also dependent to the cell spacing: 2.50 × 2.50 μm^2 as minimum, 5.00 × 5.00 μm^2 as typical and 10.00 × 10.00 μm^2 as maximum.

A1-2.1.2 *Dots* — A cell shall consist of a single spot if binary value of the cell is one (1).

A1-2.1.2.1 Shape of the dot is dependent to means to write data matrix code symbol; it may be protrusion, hollow, material/density/phase difference, combination of convex in concave circle or square, and so on. Even if the shape is somewhat complicated, a cell shall have just one or no spot depending on its binary value.

A1-2.1.2.2 The length of each dot along the surface of the article to be marked should be 4.80 µm + 10%–20% for typical 5.00 µm call; refer to right half of Figure A1-2. The ratio of the length to cell spacing must be kept for any dot independent to call size.

A1-2.1.2.3 Dot misalignment within a cell is expected to be equal or less than 1.12 µm for typical 5.00 µm call. This ensures that a minimum size dot covers a cell central area of radius 0.8 µm. The ratio of this maximum misalignment amount to cell spacing must be kept for any dot independent to call size.

A1-2.1.3 *Border* — A dot matrix code symbol has a couple of border rows and columns. One of the border rows is referred to as primary border row and the other is called as secondary border row here. One of the border columns is referred to as primary border column and the other is called as secondary border column here.

A1-2.1.3.1 The primary border row and the primary border column shall contain a dot in each cell. They are used by the code reader to determine the orientation of the matrix.

A1-2.1.3.2 The secondary border row and column shall contain dots in alternating cells; refer to Figure A1-3.

A1-2.1.3.3 The reference point shall be the physical center point of corner cell common to the primary border row and the primary border column.

A1-2.1.4 *Surround* — Surrounding area of dot matrix code symbol shall be kept quiet to identify the mark without confusion and to prevent damaging elements of semiconductor device dice.

A1-2.1.4.1 A dot matrix code symbol shall have at least a couple of rows and columns with blank cells outside of boarder rows and columns respectively, including their intersections.

A1-2.1.4.2 To allow possible disposition provided by such factors as alignment and/or positioning error for writing tool or unit up to maximum ±10% of symbol size, the mark shall be written at least 10% of the size of data matrix code symbol apart from any such members as elements, electrodes including connecting components, essential part of isolation field: 10 µm for 5.00 µm cell data matrix code symbol.

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A1-2.2 The following table shows the summary of above requirements:

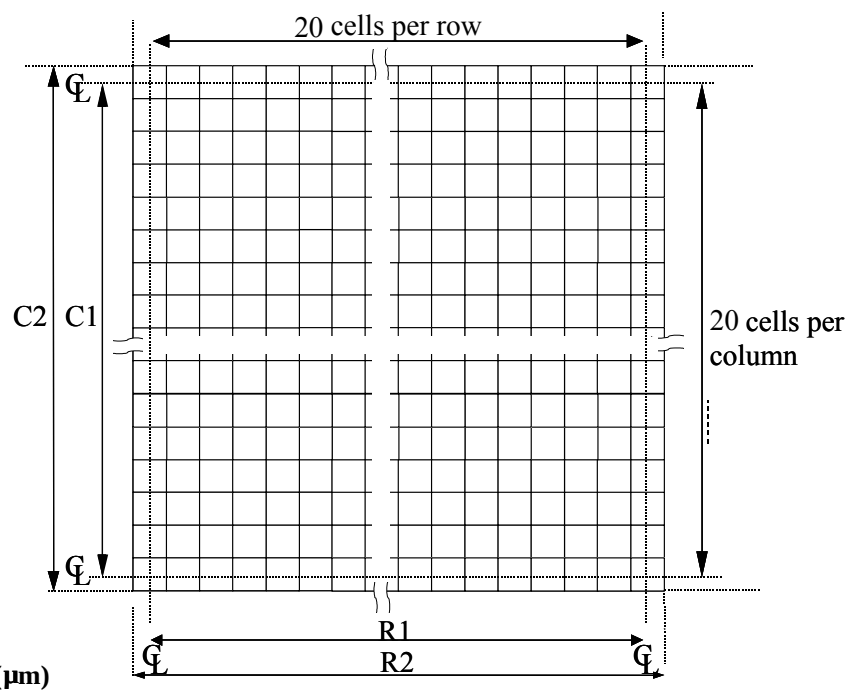
Table A1-1 Mark Dimensions of DDM

Specification Parameter	*Mnemonic Letter*	*Definition*	*Example*	*Requirement*
Cell Spacing, µm	A	$2.5 \le A \le 10.0$	5.0	Mandatory
Cell Size, µm × µm	S	A × A	5.0 × 5.0	Ruled by above
Cells per Row	R	20	20	Mandatory
Cells per Column	C	20	20	Mandatory
Field Width *R*2, µm[#1]	W	R × A ± 6%	100.0 ± 6.0	Mandatory
Field Height *C*2, µm[#1]	H	C × A ± 6%	100.0 ± 6.0	Mandatory
Quiet Zone, µm	Q	2A	10.0	Mandatory
Dot Size, µm	D	0.96A + 10, −20%	4.80 + 0.48, −0.96	Recommended[#2]
Min. Dot Misalignment in Cell, µm	M	0.224A	1.12	Mandatory
Minimum Buffer Width, µm	T	0.1W	10.0	Recommended[#3]
Minimum Buffer Height, µm	G	0.1H	10.0	Recommended[#3]

#1 The dimensions R1 and C1 between the centerlines of the outermost rows and columns are equal to the dimensions R2 and C2 minus the cell spacing. See figures A1-1 and A1-2.

#2 It depends on capability of reading device. As long as reading users of corresponding semiconductor device approve, this value may not be strictly complied.

#3 It depends on accuracy of writing equipment. As long as the accuracy is enough including recognition of essential components on corresponding device, this value may not be strictly complied.



Typical Dimensions (µm)

R1 = 95.00 ± 6% C1 = 95.00 ± 6%
R2 = 100.00 ± 6% C2 = 100.00 ± 6%

Figure A1-1
Data Matrix Field Dimensions of Typical Case of DDM (ECC200 – 20 rows × 20 columns)

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