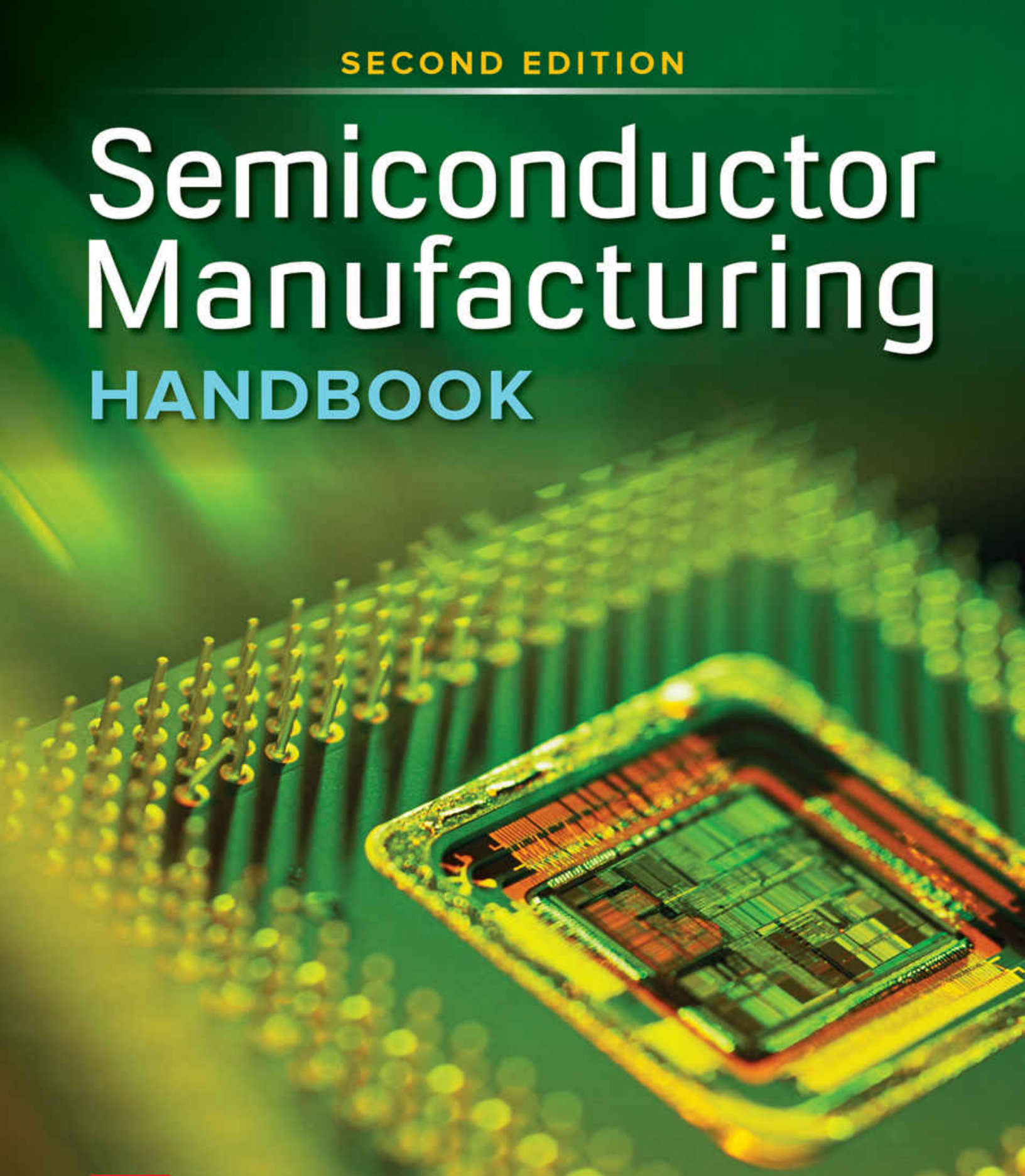
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Palo Alto, California

Second Edition



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To our mothers who cradle the world

To our earth that gives us life

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Foreword

Information technology (IT) has had dramatic social and economic impact in our global society, as continual advancement in semiconductor integrated circuit (IC) manufacturing technology has enabled ever-greater capacity for electronic information processing and storage at ever-lower cost per function. Key to the exponential growth of the IT industry over the past 50-plus years has been the steady miniaturization of the transistor (the basic component of an IC) to enable greater degrees of integration and hence greater IC functionality. The most advanced semiconductor chips today comprise over 10 billion transistors, with features that are finer than 10 nm. The fabrication process for such sophisticated products involves hundreds of steps, each requiring very high precision and/or ultrapure gases and chemicals. Impressive economies of scale make chips affordable: Presently the largest semiconductor “fabs” each have the capacity to process the equivalent of more than 1 million 200-mm-diameter wafers per year.

This handbook provides a broad overview of modern semiconductor manufacturing and market drivers, and detailed technical descriptions of the unit processes used today to fabricate the components and the interconnecting wires comprising an IC. Furthermore, it describes in detail manufacturing processes for photovoltaic devices, large-area electronics, and flexible electronics, which are proliferating as we enter the age of ubiquitous computing. The final sections of this comprehensive reference cover logistical aspects of semiconductor manufacturing, including cleanroom design, handling of gases and chemicals, process control, and factory automation.

This expansive volume is the fruit of Hwaiyu Geng’s labor of love to rally 70 leading semiconductor manufacturing professionals from across the world, whose collective experience and expertise span the breadth of the

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industry, to archive their expert knowledge. I hope that you will benefit from this tremendous effort.

TSU-JAE KING LIU, PH.D.
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Member, U.S. National Academy of Engineering

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Preface

As engineers, managers, researchers, professors, or students, we are all facing increasing challenges in a cross-functional environment. For each manufacturing problem or project, we must ask these questions: What are the unknowns, available data, conditions, and feasible alternatives to validate and find an optimum solution plan? How does one apply technical knowledge to assemble a solution plan, to support a team, and to lead and implement a project successfully?

Our challenges may include establishing microchip manufacturing processes for new products, implementing automated manufacturing processes, improving manufacturing yield, expanding capacity, or establishing quality and safety programs. A good understanding of how to manufacture microchips, as well as how it relates to other processes, will enable one to plan, design, and implement a project successfully.

The goal of *Semiconductor Manufacturing Handbook* is to provide readers with essential technical knowledge needed to work in a semiconductor fab, and the skills to establish manufacturing processes, solve problems, and improve production lines in a microchip fab. This handbook embraces both conventional and emerging microchip manufacturing technologies and includes the following parts:

Part 1 covers semiconductor fundamentals and IoT/data analytics, nanotechnology, FinFET fundamentals, MEMS fundamentals, and 3D IC design.

Part 2 gives front-end-of-line processes that include epitaxy, microlithography, etching, ion implantation, physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, chemical mechanical planarization, and AFM metrology.

Part 3 offers back-end-of-line processes that cover wafer thinning and singulation, packaging, bonding, interconnects reliability, and automatic test

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equipment.

Part 4 discusses flexible hybrid electronics, printed electronics, 3D interconnects in flexible electronics, flat-panel and flexible display technology, and photovoltaics fundamentals.

Part 5 covers gas distribution systems, ultrapure water fundamentals, process chemical handling and abatement, chemical and slurry handling, and filtration.

Part 6 reviews operations, equipment, and facilities that cover yield management, CIM and factory automation, manufacturing execution systems, advanced process control, airborne molecular contamination, ESD controls, plasma processing, vacuum systems, cleanroom design and construction, and vibration technologies.

This handbook covers topics ranging from wafer processing, final manufacturing, flexible hybrid electronics, and large-area electronics to wafer fabs and cleanrooms, contamination control, and operations management systems. The book covers the breadth and depth of semiconductor fundamentals and manufacturing technologies, and it is a useful and enlightening resource for all semiconductor professionals. This Second Edition of *Semiconductor Manufacturing Handbook* is the most comprehensive single-source guide ever published in its field.

HWAIYU GENG, CMFGE, PE

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Semiconductor Manufacturing Handbook is a collective effort by an international community of scientists and professionals comprising 70 experts from 9 countries around the world.

I am very grateful to the members of the Technical Advisory Board for their diligent reviews of this handbook, confirming technical accuracy while contributing their unique perspectives. Their guidance has been invaluable in ensuring that the handbook can meet the needs of a broad audience.

My sincere thanks go to the contributors who took many hours from their busy schedules and personal lives in order to share their wisdom and deep experiences.

Without the Technical Advisory Board members and the contributing authors, this handbook could not have been completed. This collective effort has resulted in a work that adds value to the semiconductor and Internet of Things communities.

Special thanks go to Professor Tsu-Jae King Liu at University of California, Berkeley, for her sincere and continuous encouragement to improve the handbook.

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PART 1

SEMICONDUCTOR MANUFACTURING FUNDAMENTALS

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Chapter 1
Semiconductor Manufacturing, the Internet of Things, and Sustainability

BY
HWAIYU GENG *Amica Research, Palo Alto, California*

1.1 INTRODUCTION

At the end of 2016, with a world population at 7.4 billion, there were 8 billion connected devices globally.[1] In the following decades, the Internet of Things (IoT), a subset of cyber-physical systems or CPS, would connect more things around the world exponentially. With increasing processing power, reducing costs and sizes of microchips, microchips are well recognized for the advancement of electronics technology that drive the IoT with phenomenal growth and have transformed almost every facet of daily life.

"Half a century ago, a young engineer named Gordon E. Moore took a look at his fledgling industry and predicted big things to come in the decade ahead. In a four-page article in the trade magazine *Electronics*, he foresaw a future with home computers, mobile phones, and automatic control systems for cars. All these wonders, he wrote, would be driven by a steady doubling, year after year, in the number of circuit components that could be

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economically packed on an integrated chip,"[2] written by Dr. Chris Mack in IEEE's *The Multiple Lives of Moore's Law*.

In IEEE's Special Report titled *50 Years of Moore's Law*,[3] "Moore's law has driven technology forward at a staggering clip. We have all benefited from this miraculous development, which has forcefully shaped our modern world. In this special report, we find that the end won't be sudden and apocalyptic but rather gradual and complicated. Moore's law truly is the gift that keeps on giving—and surprising, as well."

1.2 MOORE'S LAW

Dr. Gordon Moore, a visionary engineer and innovator who cofounded Intel Corporation with Robert Noyce on July 18, 1968, forecasted a bright future of electronics that integrated electronic circuits would become less costly and more powerful over time. On April 19, 1965, 3 years before he cofounded Intel, he predicted the number of transistors on a silicon chip would double every 12 months. Moore's law is updated in 1975 that the number of transistors on a chip would double every 18 to 24 months.

In an interview with IEEE, Moore stated, "I used to give talks about how other industries might have progressed. You know, had the auto industry made progress at the same rate [as silicon microelectronics], you would have gotten a million miles per gallon of fuel, and cars that could go several hundred thousand miles an hour." Intel® 4004 processor, the first general-purpose programmable processor, was built in 1971 and contained 2300 transistors. Fast forward to 2015, the 5th Generation Intel® Core™ Processor is a 14-nanometer (nm) technology with 1.3 billion transistors inside. Comparing to the 4004 processor in 10,000 nm, Intel's 14-nm chips can deliver 3500 times the performance at 90,000 times the efficiency, and at 1/60,000th the cost.[4,5]

"No exponential ever goes on forever without some kind of disaster happening at the end. Sure it has a limit," Gordon Moore said. "Materials are made of atoms, and we're not too far from where that starts to bite us."[6] Miniaturization may be slowing down. But, through invention and innovation, there are derivative technologies such as micro-electric-mechanical systems (MEMS), flexible and printed electronics, light emitting diodes (LED), photovoltaic solar, silicon photonics, etc., bringing benefits that improve our living standards and sustainability. Those technologies play

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vital roles in the age of Internet of Things. Moore's law will proliferate and continue on for many years to come.

1.2.1 FinFET Extends Moore's Law

The joint work of UC-Berkeley's Professors Chenming Hu, Tsu-Jae King Liu, and Jeff Bokor created the fin field effect transistor (FinFET) technology. King Liu describes the FinFET "as a vertical transistor, kind of like a skyscraper. Conventional transistors, called MOSFETs (metal-oxide-semiconductor field-effect transistors), are fabricated along the surface of a silicon wafer, making them flat and low. FinFETs, by contrast, are fabricated along the sidewalls of a narrow, vertical fin etched into the surface of the wafer. That means they take up far less real estate, enabling a trillion transistors to be packed onto a chip."

This unusual transistor design can scale down a gate length, the distance between the source and the drain, of less than 10 nm. A smaller gate length shrinks the transistor overall and enables it to switch on and off quickly with a higher current density. Five-nanometer FinFET designs are feasible and without significant modifications to the fabrication process. "Below five nanometers, you can have quantum mechanical tunneling and confinement effects," says King Liu, "That means small variations in manufacturing would result in large changes in performance." The FinFET transistor structure revitalizes Moore's law by freeing planar FET from the short-channel effects that limit device scalability (Fig. 1.1).[7,8]

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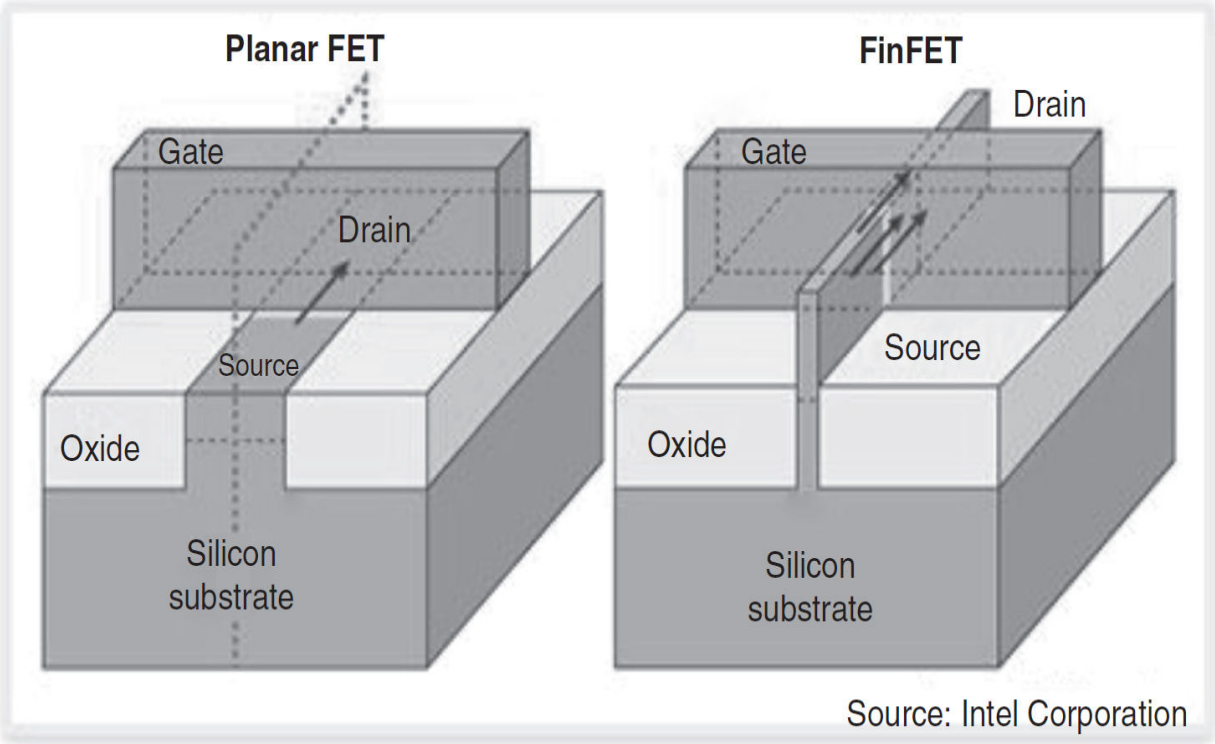


Figure 1.1 Planar FET versus FinFET.

1.3 INTEGRATED CIRCUITS AND DESIGN

The integrated circuit (IC), or microchip, was invented by Jack Kilby in 1958. There are many types of microchips. Microprocessors are logic chips that are used to perform computations (binary codes, logic gates, Boolean algebra, etc.). Memory chips, such as NAND (Not AND), store data. Analog chips operate over a continuous range of signal. Analog chips can be subdivided into linear IC and radio frequency IC. Digital signal processors convert between analog and digital signals. Application-specific ICs (ASICs) are customized chips for a special purpose. They are used in cars, televisions, digital cameras, or appliances and more.[9]

Based on a microchip's feature and development plan that encompasses use, power, area, cost, time to market, an IC's function and performance are determined and the logic circuit is designed. During logic circuit design, a logic circuit diagram is drawn to determine the electronic circuit required for performing requested functions. Once the logic circuit diagram is complete, simulations are performed multiple times to test the circuit's operation. If

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there is no issue with the operation, the actual layout pattern for the devices and interconnects is designed by computer-aided design (Fig. 1.2).

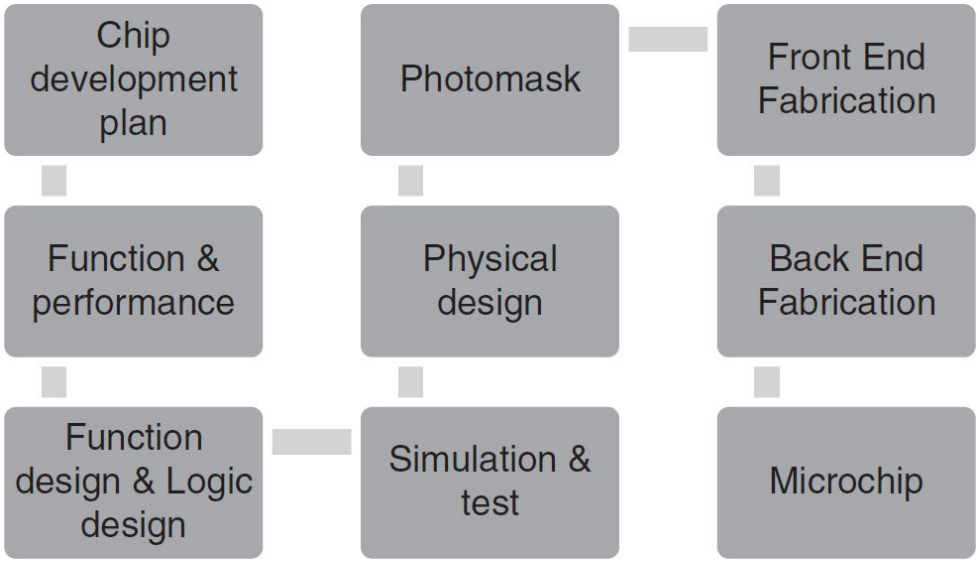


Figure 1.2 IC design and fabrication. (*Courtesy of Amica Research*.)

1.4 HOW A MICROCHIP IS MADE

A sophisticated processor can contain hundreds of millions or billions of transistors interconnected by fine metal wires. The process of making chips is extremely complex requiring hundreds of precisely controlled steps.

The base material of microchips is silicon. Silicon is called a semiconductor that relates to its molecular structure. Silicon can conduct electricity under certain conditions and nonconductive under others. This feature acts as a basic circuit of a transistor: an on/off or binary 1/0 switches either allowing or preventing electrical current to pass through a gate. The process of manufacturing microchips building millions or billions of transistors on an IC chip makes it phenomenally precise and complex.[10]

The process of manufacturing microchips includes following three main processes: (1) wafer manufacturing (2) front-end of line processing, and (3) back-end of line processing.[11–14] A microchip is formed by more than hundreds repetitive operations during front-end of line processing (Fig. 1.3). The process of manufacturing IC chip is supported by advanced manufacturing technologies that encompass material handling automation, computer-integrated-manufacturing, advanced process control, manufacturing execution system, etc.

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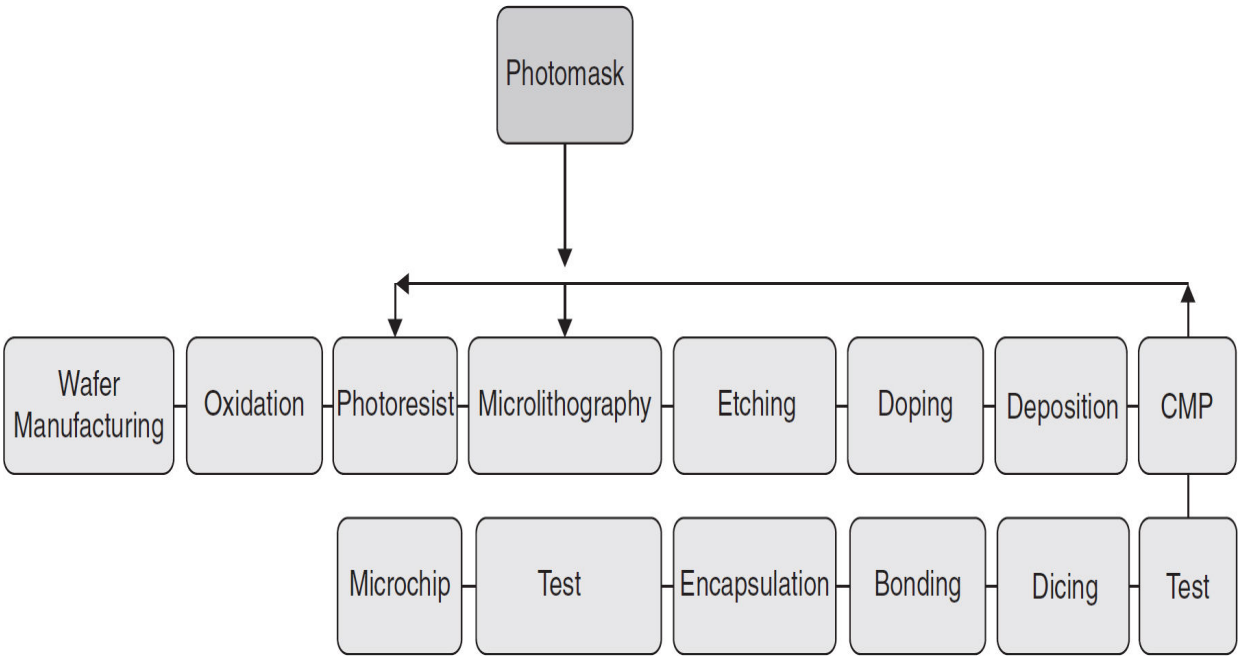


Figure 1.3 Wafer manufacturing, photomask, front-end of line process, and back-end of line process. (*Courtesy of Amica Research*.)

In the fabrication of IC, wafer serves as a substrate for IC to build-on. Many steps in front-end processing, including oxidation, photolithography, etching, doping, deposition of various materials, are built over the wafer in accordance to the IC design. Inspection and testing are also included in each step of the processes. Finally, the dies are cut, packaged, tested, and ready to be used.

1.4.1 Wafer Manufacturing

A wafer, also called a slice or substrate, is a thin disc (about thickness of a credit card) made of silicon, or other semiconductor materials such as GaAs. Silicon, the principal ingredient in beach sand, is the second most abundant element in the earth after oxygen. Before it can be used in semiconductor manufacturing it is refined to nearly 100 percent pure.

SILICON INGOT

Semiconductor manufacturing begins with a silicon ingot. Silicon ingots could be made by Czochralski (CZ) process and float-zone process. Float-zone wafers are generally not larger than 150 mm due to limit of surface tension during growing process. Most crystal ingots are grown by the

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Czochralski method. This method begins by a piece of crystal of silicon, called *seed*, is lowered in the near 100 percent pure molten silicon in crucible. The seed and crucible are rotating in opposite direction while heating purified silicon to 1200°C in an argon atmosphere. The silicon seed is slowly withdrawn from molten liquid. Silicon atoms attach to the seed, resulting in a long crystal rod or ingot, grows with a diameter of most commonly 200 or 300-millimeter (mm) across in careful control of temperature, atmosphere, and pressures. It produces electronic grade silicon that is semiconductor manufacturing quality with silicon purity to 99.9999999 percent.

WAFER FABRICATION PROCESS

A series of operations is performed to prepare silicon wafers from a silicon ingot.

Cropping, Grinding, Slicing The ends of single crystal ingot are cropped using a single-bladed diamond saw with water coolant. The ingot is then ground to a uniform diameter and the ends are chamfered to reduce the possibility of shattering the ingot. The crystal structure is determined by x-ray diffraction. A longitudinal flat section is produced by wet grinding to indicate crystal orientation of the ingot. Ingots are sliced into discs or called substrates.

Lapping After slicing, the wafers are mechanically lapped under pressure on both sides of the wafer in order to achieve flatness and parallelism. Lapping operations will remove the surface silicon which has been damaged by the slicing process and thin the wafer to desired thickness. The edge of the individual wafer is rounded by the use of wet automatic grinders.

Etching Wafer dicing and lapping degrade the silicon surface crystal structure, so wafers are etched with a solution containing nitric, acetic, or hydrofluoric acids in order to remove external damaged surface and reduce the thickness of the wafer. Etching operation could be done in manual etch tanks or automated etching machines.

Polishing After etching, the wafers are polished to a super-flat, flawless, and mirror-smooth surface with remaining roughness at atomic scale. Polishing process is usually completed in two or three polishing steps. Wafers are mounted onto a metal carrier plate that is attached to the polishing machine by vacuum. The polishing process combines with

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pressure mechanically and chemically using fine slurry such as Al_2O_3, SiO_2, or CeO_2.

Cleaning Finally, the wafers are cleaned to remove any particles on the surface of a polished wafer thereby making the wafer residual free. Variable ultrapure chemicals could be used for cleaning that include ammonia, hydrogen peroxide, hydrofluoric acid, hydrochloric acid, and deionized water.

1.4.2 Front-End of Line Processing

Building circuits on a wafer is an extremely complex and precise process. The process consists of hundreds of precisely controlled steps with as many as 30 layers of complex circuitry. Chips are built, taking from 10 to 30 days or more, in specific patterns and recipes to produce hundreds or thousands of die on each 300-mm wafer.

The process of making IC chips is called fabrication. The factories where chips are made are called fabrication facility or fab. In a fab, there are cleanrooms where fabrication in batch of wafers is built. Because particles of dust can ruin the complex circuitry on a chip, purified air is constantly recirculated in a cleanroom. For a class ISO 1 cleanroom, a cubic meter of air contains no more than 10 particles, measuring 0.1 micrometer or µm (millionth of a meter). Fab technicians wear bunny suits that are specially designed to keep contaminants off the wafers during fabrication.[15,16] The following are operations in the Front End of Line Processing (FEOL).

EPITAXY

Epitaxy is one of the fundamental processes used to make semiconductor devices. Epitaxy refers to deposit an overlayer of a crystal (epitaxial film) on a host crystal (substrate) in an ordered fashion. It is desired that the overlayer has a defined orientation with respect to the substrate. The epitaxial film and substrate could be same or different materials. There are three types of epitaxy: liquid phase, vapor phase, and molecular beam epitaxy.

OXIDIZATION

Silicon oxide (SiO_2) serves as an electrical insulator that is a key component in IC circuit. Growth of oxidation can be achieved by dry or wet oxidation.

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Oxidation is a diffusion process. Silicon wafers are first heated and exposed to ultrapure oxygen at elevated temperatures in a diffusion furnace. By carefully controlled conditions in the furnace, a silicon oxide (SiO_2) film, dry oxidation, with uniform thickness is growth from the SiO_2/silicon interface.

$$Si + O_2 \rightarrow SiO_2$$

Wet oxidation is preferred to dry oxidation for growing thicker oxide at a faster rate. Wet oxidation is performed by exposing the wafer to ultra-high-purity water vapor or using hydrogen and oxygen which are burned in a torch flame to form ultra-high-purity water vapor in an oxidizing furnace.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

PHOTOLITHOGRAPHY

Photolithography is a process by imprinting a specific IC design pattern on a wafer. Before performing the photolithography process, a photomask (reticle) is prepared. A photomask has a copy of the circuit pattern drawn as an opaque pattern on a quartz plate. A quartz plate is first polished in high precision. The quartz substrate is then coated with a thin layer of chrome material by sputtering that is opaque to UV wavelengths. A photosensitive chemical called resist is spin-coated over the chrome photomask blank. Then a circuit design pattern is transcribed into the chrome film by electron beam lithography. After exposure, develop and etch, the photomask blank becomes a photomask with a copy of the circuit pattern.[17,18]

Photoresist Application A wafer is coated with a light-sensitive liquid called *photoresist*. By pouring a small amount of the photoresist to the center of the wafer while the wafer is spinning at high speed, the material will spread over the entire surface in a thin, uniform coating. The photoresist material is sensitive to “photo” (light) and it “resists” certain chemicals that are used to remove portions of the material below the photoresist.

Photomask and Exposure A photo aligner precisely aligns the photoresist-coated wafer to the photomask. The photomask, acting like a stencil, contains the pattern to be imaged onto the wafer. The aligner projects light through the photomask and optical reduction lenses to the wafer. This results in exposure to the photoresist in areas where not protected by the

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mask. For a positive resist, the areas exposed to light undergo a chemical reaction that will make the photoresist soluble in an alkaline solution (developer). A negative resist becomes insoluble in regions that expose to the light. The exposure tool repeats the process across the wafer to form the same image throughout the wafer. The yellow lighting is necessary in photolithography rooms to prevent unwanted exposure of photoresist to artificial light.

Resist Development and Hard Bake After exposure, a wafer is developed with aqueous solutions of either sodium hydroxide or potassium hydroxide. The developer is applied by either immersion, spraying, or atomization, causing the exposed areas of the photoresist to be dissolved and removed. This leaves a photoresist pattern similar to that depicted on the photomask.

Following resist development, an additional baking process, or "hard bake," is performed to harden the remaining photoresist. The photoresist can now protect the underlying material during etching.

ETCHING

The etching process removes layers of silicon, silicon oxide, polysilicon, or metals according to the patterns from mask. Etching can be done by a chemical solution (wet etching) or plasma (dry etching, reactive-ion etching).

Wet Etching Wet etching is a simple technology. It is accomplished by submerging wafers in chemical bath. Wet etching is usually isotropic with etching progressing equally in all directions that will cause undercutting of the mask layer by the same depth as desired area. Therefore, consideration of selectivity is important. Selectivity is the ratio of two etch rates: the rate for the layer to be removed and the rate for the mask layer to be protected.

Dry Etching Dry etching is one of the most used processes in semiconductor manufacturing. Dry etching may be anisotropic (direction dependent) that allows effectively etching desired surfaces or layers through the use of chemically reactive gases, or through physical bombardment of argon atoms.

Reactive ion etching (RIE) is a dry etching technology that combines chemical and physical etching. A wafer is placed in a vacuum chamber reactor. By applying radio frequency energy to a gas containing a chemically reactive element etchants, such as fluorine-based or chlorine-based gas, the

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plasma releases positively charged ions. The ions strike or bombard the wafer surface vertically to etch or remove materials which are then removed by the vacuum system.

After etching, the resist has served its purpose and could be removed from an etched wafer by oxygen plasma.

DOPING

Intrinsic semiconductors, such as silicon, can be doped with extrinsic atoms in order to increase their conductivity. Doping can be achieved either by ion implantation or diffusion.

Ion Implantation Materials used for doping intrinsic semiconductors are typically ionized atoms or molecules for silicon with valence 4, either 3 or 5 valence electrons, such as boron or phosphorous. The dopants are accelerated in intense electrical fields to an energy ranging from sub-keV to multiple meV, and bombard the surfaces of a wafer, where not masked or exposed by etching processes. Upon striking the wafer, the dopant is embedded at various depths and precise locations within the bulk, thereby altering the dominant carrier concentration of the bulk material to p-type (hole) or n-type (electron). Ion implantation introduces damage into crystalline substrates, and a high-temperature annealing step, 800 to 1200°C for tens of seconds to 30 min, will restore the crystal structure and further incorporate the dopant atoms into the crystal lattice.

Diffusion Diffusion is a term that can be used to describe the introduction, placement, and/or activation of dopants to semiconductor in a furnace. Sources of dopants could be in gaseous, liquid, or solid form. Gaseous dopants are most widely used that include arsine (AsH_3), borane (BH_3), phosphine (PH_3), etc. Dopants move in semiconductors as a result of a concentrated gradient. Fick's laws of diffusion are equations that describe how dopant's diffusivity, concentration, temperature, and time relate in determining the dopant profile in silicon. The diffusion of dopants limits the thermal budget and processing temperatures of more advanced IC integration.

DEPOSITION

Thin film deposition processes place thin and uniform materials such as silicon nitride, silicon dioxide, silicon, or metal onto wafers. The silicon

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layers are formed as an insulator. The metallic layers are formed and used in the wiring of the circuit. Some commonly used thin film depositions are physical vapor deposition (PVD), chemical vapor deposition (CVD), or electrochemical deposition (ECD).

Physical Vapor Deposition Physical vapor deposition (PVD), a method of sputtering, is performed in a high vacuum chamber. The source material (sputtering target) and the wafer substrate are connected to a high voltage power supply. When sputtering gas (an inert gas such as argon) is admitted in the chamber, argon gas is ionized and creates a plasma between sputtering target and wafer. The argon ions are accelerated and bombard the sputtering target that creates impacts knocking off target atoms or molecules. The target atoms or molecules then travel through vacuum to the wafer, where a desired thin film is formed.

Evaporation is another PVD process. First, wafers are placed in a vacuum chamber, the gases in the chamber are removed using a vacuum pump. Once the chamber is free of residual gases, the source material (metal) is heated to cause it to evaporate. The evaporated molecules are dispersed and landed on the wafer and formed a desired thin film.

Chemical Vapor Deposition Chemical vapor deposition (CVD) is a chemical process that can be accomplished in a vacuum (low pressure CVD or LPCVD) to produce high quality, high performance, large area films. Importantly, CVD is often used to provide highly conformal film coatings on trench walls and bottoms as the sizes of such features continue to shrink.

Reactant gases, or precursors, are introduced into a reaction chamber that contains wafers. In a hot-wall reactor or plasma environment, reactive species are created at the reactor walls or in the plasma, and then diffuse to the wafer surface, where film growth can take place. This is known as a homogeneous process, as reactive species are formed in the gas phase. In a cold wall reactor, the reaction energy is supplied by heating the wafer, and reactive species are created by interaction with the wafer surface—a heterogeneous process.

Atomic layer deposition (ALD) is a special type of CVD that deposits a single layer of a film each time in a tightly controlled process.

Electrochemical Deposition Electrochemical deposition (ECD) is used to deposit a thin metal layer, which will form interconnects (integrated wires) connecting various devices on an IC. ECD is an electroplating process. The substrate is submerged in electrolyte solution and serves as a

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cathode (negative side of power supply). A copper electrode serves as an anode (positive side of power supply) forming a circuit through electrolyte solution. The copper ions are reduced on the cathode or substrate and form a film.

CHEMICAL MECHANICAL PLANARIZATION

A flat surface is required for IC processing, such as photolithograph operation. There are several ways to perform planarization. Chemical mechanical planarization (CMP), by applying abrasive chemical slurry and mechanical force (polishing pad), is one of the best planarization techniques that polishes away excess material left from previous processes and planarizes the uneven surface to create a flat surface. The depth-of-field requirement is down to angstrom level.

REPEAT THE STEPS

There are typically over 350 process steps required to make a microchip.[19] Replicating the steps photolithography, etching, doping, deposition, CMP layer by layer until the last layer is formed. The wafer with transistors and interconnects is moved to the back-end of line processing.

1.4.3 Back-End of Line Processing

Back-end of line (BEOL) starts with testing a wafer with transistors and interconnects. An automatic, computer-driven electrical test system checks the functionality of each chip on the wafer. Chips that do not pass the test are marked with ink for rejection. The wafer is then diced into individual die. Individual die is bonded with wires, assembled, tested, and finally packaged.

GRINDING (THINNING) AND DICING

The wafer is first attached by a protection tape, called back-grinding tape, to protect device layer of the wafer. The wafer is turned over and the back of the wafer is ground (thinning) to suitable thickness that would accommodate assembling and packaging.

Dicing, or singulation, is a process cutting semiconductor wafer into individual die. After thinning, the wafer is mounted on a dicing tape frame with device side upward. A disc blade with diamond grains cut the wafer

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into separated dies. The dicing process could be done by diamond blades, laser ablation, or stealth dicing.

WIRE BONDING

Wire bonding is a process to connect IC to the substrate. Wire bonding uses very fine gold or copper wire to connect a die to the substrate or leadframe by ultrasonic or thermosonic techniques. Ball bonding is the most popular interconnect method. The formation of ball bonding starts on the chip, the wire loop, finally the bond on the substrate. Wire bonder is a fully automated machine with high-speed, high-precision servo system, an ultrasonic transducer for bonding operations, and an automatic vision system for device alignment.[20]

PACKAGING AND ASSEMBLY

IC packaging, or encapsulation, is performed to contact and encapsulate semiconductor material in a supporting case, or package, with mostly molding resin. The package is to support IC performance by keeping IC from hostile environment, handling thermal management, and providing a reliable interconnect to the substrate which is mostly a printed circuit board or PCB, which combines a multitude of ICs and passive components to build a microelectronic system. There are packages for single chips but also for multiple dies which is referred as an MCM (multichip module) or a SiP (system in package). After packaging, printing, or engraving product information by laser is performed onto the package surface or onto the backside of the chip. Most of the packages are soldered or glued onto the substrate.

FINAL TEST

The packaged IC chips are ready to use. However, there are many things can go wrong: die may crack during assembly, bonding wires may be poor or not connected, ICs may be affected by static discharge due to poor handling and other issues. So, the IC chip is individually tested on a tester. The chips are tested for functionality, performance, and power according to a test program prepared specifically for each type of IC in advance. In many cases these test programs are a variation of the ones used in wafer sort.

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