

SMC-WP-004
APRIL 1997

SURFACE MOUNT COUNCIL WHITE PAPER

Design for Success



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The Surface Mount Council (SMC) is made up of key industry representatives from EIA, IPC and SMTA. The SMC is dedicated to promoting the use of surface mount and advanced electronic packaging technology in the design and production of electronic hardware.

Council Members represent user, supplier and equipment manufacturing companies engaged in surface mount implementation for automotive, telecommunication, computer, instrument, government, consumer and medical electronics.

The mission of this Council is to facilitate, coordinate and promote the orderly implementation of surface mount technology through standardization, the development of technical documents and other means.

This Technical Report is a compilation of six papers. The focus is to establish the design for excellence parameters for designing and fabricating electronic assemblies. The presentations were commissioned by the SMC and prepared by the industry experts indicated under the title of each presentation.

The papers were presented as a part of the Surface Mount International proceedings. They have been extracted to provide the reader with a compendium of the major conclusions that should be observed in order to follow Design for Excellence Principles.

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REENGINEERING NEW PRODUCT DEVELOPMENT PROCESSES TO INCORPORATE DESIGN-FOR-EXCELLENCE (DFX)

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ABSTRACT

This paper addresses the complete process of reengineering New Product Development Processes to incorporate DFX methodologies. The companion papers address specific aspects of DFX such as Fabrication, Assembly, Test, Reliability and the Environment. Issues like Serviceability, Repairability, ESD protection, etc. are not discussed but are equally important. The paper presents the case for a comprehensive analysis of the key business issues and definition of requirements before initiating work to refine or restructure processes. The specific tools, methodologies, and practices of DFX are often the easier elements to address and implement. Short and long term success requires a base of robust business and management processes. The paper addresses the importance of assessing the global competitive situation and defining the specific requirements for success of the individual organization. Comprehensive corporate and functional strategies, roles of individuals and functions, specific criteria of success, and other requirements are discussed. The need for effective and stable leadership, business focus and management is presented. Tools and methodologies required to meet the "Design for": criteria are presented as elements to consider in refining or redesigning new product development processes.

A very effective and proven process is presented to reengineer the product or business processes. It is easy to learn, implement, and use. The methodology focuses on the specific business objectives and requirements. It requires the active involvement of a key individual from each functional area and in a very short time produces the optimum solution for the particular objectives addressed. Individuals from the functional organizations develop the detailed processes. It embodies all the issues that the functions and individuals want to address and assures comprehensive and robust designs. Solutions are sought that provide significant competitive advantages. They are based upon the information available from benchmarking, industry best practices, DFX practices, and innovative solutions discovered during the process. Specific tasks, assignments, and a step by step process to implement the new process are developed by the people that own the responsibility to carry out the improved process. The people can then define the optimum organizational structure to effectively implement the resulting product development or product and process design process. Typical results and benefits are presented.

INTRODUCTION

The fundamental measures of success for any business are economic. The Electronics Industry has provided rapid improvements in technologies and capabilities that have provided enormous benefits. Global markets have responded with major increases in demand for all types of products. The demand provides the profits and capital required to support the tremendous growth. The future also contains major growth potential in many new areas. The computer, communications, consumer electronics, and information markets are currently creating major demand. There are other markets, such as autos, that may have even more growth opportunities.

Successful electronics companies will benefit with increased orders for products and services. Those companies that can rapidly define and develop excellent products will enjoy "premium" margins. They will enhance their profits until the competition responds with competitive products that force the market prices down into cost based pricing. Companies must continually innovate and create exciting new products to be successful.

A key element for success is the ability for a company to quickly respond with very competitive, high quality, and low cost products. Although the electronics industry is one of the most flexible and responsive industries, consumer demand will probably increase the pressure for even faster responsiveness for new products during the next decade.

THE CHALLENGE AND OPPORTUNITY

This enormous opportunity presents some staggering numbers described by the projected volumes of chips. The American Electronics Association projects the World Total Electronics Market to grow at ten to eleven percent annually [1]. This was projected to be \$940 Billion for 1996. VLSI Research was quoted by the Associated Press to estimate that forty to fifty of the nine hundred IC fabs in the world should be replaced each year. Currently fewer than twenty are being replaced each year. Major capital investments are being made in fabs to meet the demand. There was an estimated \$18 billion spent for 1994.

This discussion of the macro market is presented to illustrate the market for electronic products is very, very large and growing at a rapid rate. It is to emphasize that increased

competition will increase pressure and profit margin demands upon all manufacturers. It is a market that will have major opportunities for companies that have effective new product development processes. It will strongly favor companies that have well-designed processes to apply Concurrent Engineering, DFX tools, Concurrent Manufacturing, Predictive Engineering, robust data bases and effective processes to rapidly introduce innovative high quality products.

The trend for the world electronics market could well be similar to leaders of the fashion garment industry. In this marketplace, ideas for a new product can be created on Monday. On Tuesday, the garment is designed, documented in a computer file and transmitted to multiple manufacturing sites around the world. It can be manufactured and distributed to multiple international locations by Saturday. This characterizes a mature industry that has developed a very responsive approach to consumer demands.

The computer, consumer electronic and telecommunications industry have many similarities to the fashion clothing industry. For example, there are many styles or configurations in the personal computer market for monitors, keyboards, disk drives, monitors, power supplies, main boards, etc. A quick glance at the advertisements in your Sunday newspaper illustrates the quickly changing configurations of computers, telephones, etc. These quickly and ever changing customer wants further support the need for flexibility and short time-to-market for new product development and manufacturing in the electronics marketplace.

EVERYONE WILL BE REQUIRED TO CHANGE

Competition in all markets is significantly increasing. The reductions in international barriers and free flow of business will create even more competition from sources that have definite advantages in their cost structures. Companies that are having difficulties with cost, time-to-market or other issues of their new product development process must change the processes that are developing those products.

This corporate issue quickly becomes a personal issue for people in organizations that refuse to change and improve. Consistently producing noncompetitive products, lost market share and low profits have affected too many people in our industry. The reality is that it only requires one person to have the motivation and take the leadership for creating positive change. One person or a few people can lead the change the behavior and capabilities of even the largest company. It can be done before the situation becomes terminal.

An old saying can be paraphrased to, "You will continue to get what you are now getting unless you change the processes you are using." It is very simple. Some gains and

improvements can be gained by working harder but the only real answer is to change the processes or ways the work is executed. Development processes, like all natural processes, have a certain defect rate and the process must be addressed, analyzed, and designed to minimize defects, insure positive results, and produce world class products without special attention, screening, or rework.

Change requires someone to lead the change. Managers and other key individuals in the product development process must take responsibility for creating the most effective product development processes for their particular organization. Managers own the responsibility to provide the leadership, direction and commitment to change the processes. There are some examples where individual engineers and other professionals have successfully changed the processes without management support but that should be the last resort. The actual process requires very few days of dedicated work. It is probably the most important and rewarding work that can be done within a company.

Successful products generate the revenue that fuels the company engines. Marketing, Sales, R&D, Manufacturing and all other functions require parts of this revenue to operate and develop even more products. Developing products that generate this revenue is the most important task within a company. All other activities support this process or provide direct customer support.

Change is required of everyone. The companies leading in product development must change and incorporate improvements because today's processes cannot insure future success. There are ways to smoothly incorporate new ideas, improvements, and best practices into the existing processes to remain leaders.

Companies that are in the middle of the pack need to change to prevent falling further behind. The companies that are truly behind must address changing their processes today for survival. It is not difficult to do but requires leadership, commitment, and the will to make things happen. Again, a very small group of people can cause tremendous improvements to occur.

COMPETITION DRIVES THE NEEDS FOR BETTER PROCESSES

The concepts of Design for Manufacturability, Assembly, Test or DFX have been available for many years. These concepts have always been important but not everyone has given them the same attention. Why is this any different now than in past years? It is because traditional techniques and "throw it over the wall" organizations will simply not survive in the competitiveness of the future marketplace. The competition in the market will force every company or operating unit to become competitive or they will simply cease to exist. People that don't get the message or refuse to

take action will experience tough competition in the marketplace from those people that take the initiative to act now. Reorganizations, consolidations, and down sizing are largely the result of weak and ineffective new product development processes. Many companies suffer from long periods of flat revenue and struggle for survival because of ineffective product development processes.

An open and competitive market can be very rewarding or it can be very cruel. There are many companies that seem to consistently develop winning products. However, everyone has seen companies that could not or refused to develop the capabilities to develop the processes to quickly and effectively develop new products and be competitive. Unfortunately, good intentions, management rhetoric or wishing success are of no value in the marketplace. It is also true that size is no guarantee of success. Some of the most incredible examples of organizational ineptitude exist in the largest of companies. Sometimes, the larger companies are easy targets for aggressive companies. Larger companies often have created the markets but cannot compete in the execution of competitive new products to maintain their lead.

Rapidly developing the most competitive new products is truly where small companies can take business from large companies. Many examples exist in the electronics industry where larger companies have been removed from the marketplace by smaller, well focused, well managed, and well coordinated teams of people. This is particularly possible in the electronics industry because of the abundance of excellent subcontractors, standard components and materials, good suppliers, and adequate capital.

THE ROBUST IC DEVELOPMENT PROCESS

The message is that "every" company must focus on the processes to develop very competitive new products in the shortest possible time. One element of the electronics industry that addresses the total integrated development and manufacturing processes required for success and survival is the IC industry. The processes to design, manufacture, package and test integrated circuits have all the needed elements required to develop competitive products. A critical aspect is the capability to accurately characterize the processes and predict results before the actual detailed design begins. The Integrated Circuit DFX rules are general enough to apply to nearly every product development project. They are well documented, easily understood and available to everyone to apply to new product design and development projects. These rules are easily applied and insure that substantially more competitive products are developed.

Predictive models exist to provide complete performance, yield and cost data for alternative product specifications. This completely integrated capability is available to the designers of a new chip as they are considering alternatives

of design architecture. A very key element is that the models available to the product managers, management, designers and other members of the development team can very accurately predict all the critical performance and cost parameters before the product is designed. These capabilities are not options for the IC industry. They have been developed because of the economic parameters required to make a profit, survive and be successful. The IC industry has incredible capital requirements, enormous volumes, tremendous leverage based upon process yields, and very highly refined technologies and processes. Very slight inefficiencies can quickly become life threatening and must be recognized and designed out of the processes at the very beginning.

This is the ultimate "Design for Every Important Consideration" or DFX process. Every issue that is important for IC design, development, manufacturing, packaging, and test is embedded into the models. The model accurately represents the process capabilities and the resulting costs for every step in the process. The financial models both require and reward investments to achieve this capabilities. It is a highly evolved process and a necessary element of any successful IC business.

The driving factors that require the "up-front total capability" for the IC industry do not generally exist in the electronics industry. Fortunately, or unfortunately, depending upon the perspective, companies can exist and produce products without such comprehensive and robust systems, processes, and methodologies. Electronic product manufacturing companies can and do get products out the back door by changing the product, reworking, tweaking, inspecting in quality, and otherwise brute force manufacturing products. Costs and time to make engineering changes are not so obviously prohibitive as in the IC process. The negative consequences of making changes to the competitiveness may be as serious but probably will not be noticed. This is especially true because most accounting systems do not capture and report the total impacts of these types of activities.

DFX MUST BE CONSIDERED AT THE START OF A PROJECT

The importance of making the correct decisions before actual design begins was documented by the Ford Motor Company many years ago. The results illustrated in Figure 1 illustrate that more than eighty five percent of the Manufacturing cost of a product is fixed within the first five to ten percent of the development time. The percentage is even higher for electronics and is still higher for IC's. This shows the need for a comprehensive and complete analysis of the alternatives and consideration of DFX guidelines before beginning the actual design of an electronic assembly or product.

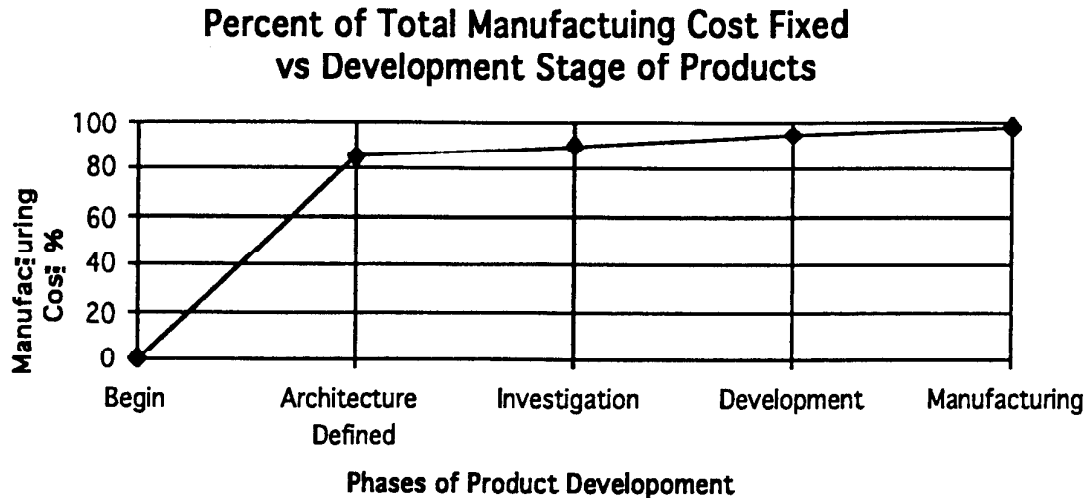


Figure 1. Percent of Total Manufacturing Cost vs. the Development Stage of the Product

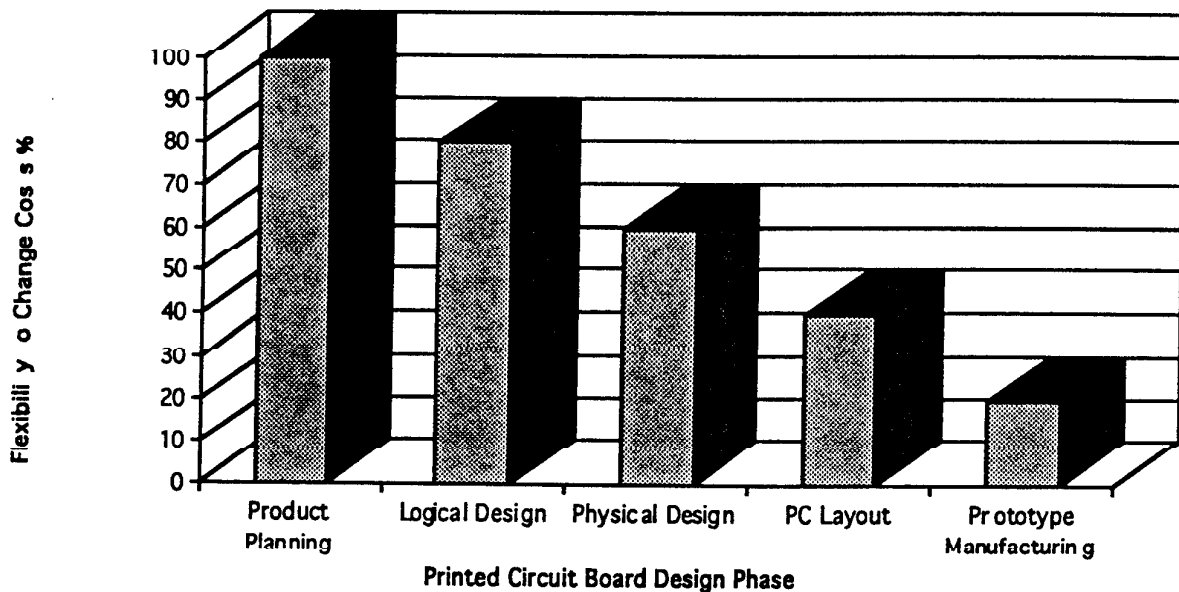


Figure 2: Flexibility to Change Costs vs the Board Design Stage

The flexibility to control costs quickly diminishes as the product is developed. This is illustrated in Figure 2.

COMPANY SIZE:

ADVANTAGE OR DISADVANTAGE?

Few product development and manufacturing organizations have the integrated and predictive processes characterized by the Integrated Circuit industry. Business research documented by Bennett Harrison in his book, Lean and Mean, describes the gains made by larger US, UK, and EEC companies compared to smaller companies [2]. While

smaller US companies have done better at product innovations, larger companies have an advantage in process innovation. A key element in the core competence for the IC industry is the integrated, robust development and manufacturing process methodologies and technologies. Product manufacturing companies that have integrated, robust and comprehensive new product development processes are likely to have definite advantages as the electronics industry matures. The dominant positions of the large Japanese and Korean VCR manufacturers is a good

example. No new VCR competitor is likely to enter into this market.

Companies that have robust development processes are likely to dominate organizations that do not develop comprehensive development processes and capitalize upon the strengths of all functions and resources. All companies must rethink their development processes and optimize them around their specific needs, resources, and market requirements. Reengineering the product development processes to incorporate the appropriate DFX methodologies will provide the smaller companies with powerful weapons in the fight to be successful.

Success requires first being competitive, consistently profitable and then the possibility of surviving. Bennett Harrison's data from three studies of all types of businesses for the US, UK and the EEC is startling. The US press and the electronics industry generally have lauded the value of small entrepreneurial start up companies for creating large numbers of new jobs. One probably would interpret this as a measure of success. Bennett Harrison's "real" data from extensive research and studies over a base of all businesses in the US shows that a great deal of the growth in the smaller companies has resulted in the "lean and mean" downsizing of larger companies.

INTERNAL AND EXTERNAL MANUFACTURING

Harrison suggests that the work is shifting from the larger product focused companies to external process focused companies, the subcontractors. This is particularly true in the computer and electronics industries where very large subcontractors have emerged for fabrication, assembly, test and distribution of products.

The economic models for these mega-subcontractors begins to resemble those of the IC manufacturers. Their process controls, predictive models, DFX rules, cost models, volumes, procurement strengths, asset utilization, process technologies, internal focus, commitment and discipline are very effective. The resulting manufacturing costs for the subcontractor plus their "reasonable profit" is still less than the "manufacturing cost" of the final Product Manufacturing Company. At least that is what the Product Manufacturer's accounting system reports. The decision makers within the Final Product Manufacturing companies agree and believe it or they would manufacture the products themselves.

Why is this discussion presented? Because the reality is that the central theme of Design for Success or DFX is rapidly changing. It is quickly becoming Design for Survival. This is because the larger focused fabrication and assembly companies have the economics and management capabilities to carve core competencies from the innards of their customers and make a handsome profit doing it. Now that they have the subassembly and assembly manufacturing

responsibility, they will and are often completing the final Product Manufacturing role. They have the competencies to compete in the Manufacturing Arena and are winning bigger and bigger pieces of the total profit pie. Their next logical step is to move down the product chain and vertically integrate forward, toward the final product. This will cause them to start competing for the actual design of the products in addition to the pure assembly and test roles.

The subcontractors now control the central data bases, DFX knowledge, and process capabilities required to effectively compete in the toughest part of the process, namely manufacturing the products. They are in a commanding position to become bigger players in the market. There are few examples in any industry where companies successfully vertically integrate towards the consumer. This is an excellent example and we can all watch it happening today.

The other reason to address this phenomenon is because the larger subcontractors must develop and commit to provide very comprehensive DFX rules to their customers. They must have consistency, commonality, and proven designs to meet their business objectives. They have in fact become very similar to the IC manufacturers and for the same fundamental reasons. It must be even more important for the internal manufacturer because they typically do not have the resources to invest in the process technologies. There is little room for inefficiencies when competing with the large refined processes of the subcontractors.

Companies competing with these major players must quickly and effectively decide how they are going to respond. The previous discussions illustrate that the market is enormous and growing. However, small and large companies are at risk if they do not respond with a competitive product development and manufacturing strategies and capabilities.

The reality is that if a company loses its internal competency to develop and manufacture products better than the competitors, it loses some of its advantage in the market place. It must share some potential profits with its subcontracting partners. It is true that the company can still maintain a competitive advantage through Marketing, Sales, and Distribution. However, it is exposed to companies that do not have the overhead burden of a larger company and that can contract out Marketing, Sales, Design, and Distribution to provide much more competitive products into the marketplace.

THE PROCESS FOR SUCCESS

The need for paying attention to the details of New Product Development is obvious. It is sometimes easier to set up some DFX tools than to address the broader issues that may have more impact upon the business. Success requires excellent management and coordination, sound Business, Marketing, Sales, and Manufacturing plans and a sound and

effective product development process. The best DFX plan will not overcome fundamental weaknesses in key strategies or product plans. This is emphasized because often the engineers and managers in the product development processes sometimes are so heavily involved in DFX programs and they ignore weaknesses in more fundamental business issues. DFX is only one of the important issues to increase the total quality of new product development. Individuals should become aware of other fundamentals that are necessary for success and act to address the issues. Development engineers are very innovative, adaptive and react to the situation to get the job done. However, the focus must be to develop a process that works every time without this extra effort.

Products developed by multifunctional teams that have created or reengineered their own optimized product development process consistently introduce products that:

- Meet Specifications
- Are Low Cost
- Have a Consistent Quality
- Have a Short Development Time
- Are Produced to Plan
- Can Provide Rapid Volume Changes
- Have a Minimum of Design Changes
- Meet Profitability Objectives

A robust new product development process is required to have the most effective DFX processes. Solid Business, Marketing, Sales and Distribution, Product Development, Quality, Technology, Financial, Cost Accounting and Manufacturing strategies are essential. The strategies should support each other. They should be clearly and openly communicated and understood throughout the organization. Strategies can vary from those of a being a technology leader, cost leader, follower, or somewhere in between. It is essential that all key managers have the same vision and objectives for operating and making decisions.

The Product Development organization needs clear and consistent direction to most effectively use DFX rules and guidelines. Understanding the customers' real needs is very important. A complete understanding of the marketplace and competitors is essential to determine and define the product features and specifications. There are many proven methodologies to define customers' needs. The results are essential to determine the market requirements, features and specifications of the products to be developed. This is particularly important to prevent false starts and restarts of the development team. Development teams generally can develop products much more quickly and effectively when stable product plans are available.

EMULATING THE IC DEVELOPMENT PROCESS

The proposal was made that the processes and methodologies available to IC designers are desirable and should be sought for electronic assembly and final product manufacturing. A comprehensive model for the process has been described in the literature [3]. This model is based upon four separate domains. They are Concurrent Design, Concurrent Manufacturing, a Product Data Manager database, and a Predictive module. The IC model previously described has all the elements in a refined software to provide sophisticated modeling and predictive capabilities for all input scenarios.

IC product development models incorporate all the elements of DFX. The IC rules have been continually developed and improved. Best practices and lessons learned have been incorporated into the processes. The appropriate metrics have been defined and the capability to facilitate what-if scenarios is available. IC design rules and procedure summarize all the DFX rules and criteria. The model described in [3] describes the data base requirements for electronic products and assemblies.

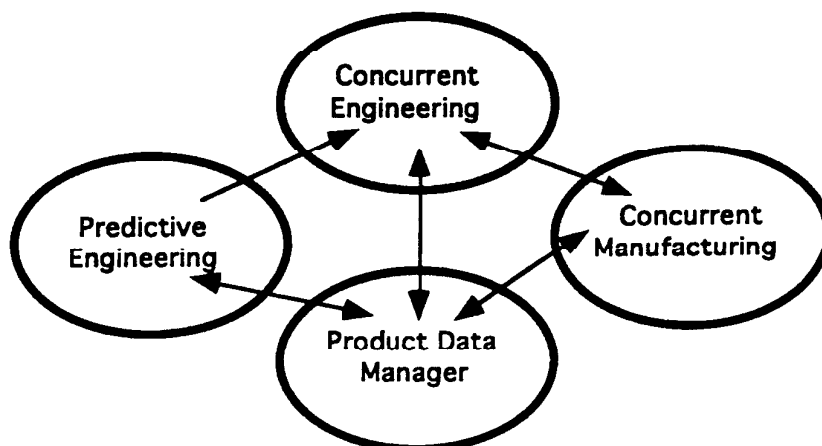


Figure 3: Organizational Architecture of a Desired Database

Examples of the information each function is responsible for are shown below:

Product Data Manager

Bills of Material
Product Structure
Engr Change Requests
Engr Change Orders
Purchase Orders
Approval forms
Electronic Approvals
Drawings
Text Files
Process Sheets
Part Data
History Files
Expert System Database
Group Technology

Concurrent Manufacturing

CAM Databases
Internal & External suppliers
Manufacturing Models
Produceability metrics & data
Process capabilities
PPM data by process & process
Mfg. rules and best practices
Process documentation
Preferred components
Preferred technologies
Preferred suppliers

Concurrent Design

PWB Design Rules
CAE Tools
CAD Tools
Performance Models
Simulation Models
Cost vs. Complexity
PCB Test Rules
Fab Test Rules
ICT Test Rules
Technology Profiles
Rework Rules

Predictive Engineering

Design for models:
Minimum Complexity
Fabrication
Assembly
Fabrication Test
ICT
Final Test
Environmental
Packaging
ESD
True Costs
Auto Router Rules and Metrics
Technology Characterizations
Materials Characteristics
Optimum Design Density
Relative Cost Indexes
SMT Assembly & Test
MCM Application Rules
Chip on Board Application
Rules
IC's Applications and Rules

TEAM MEMBERS PROVIDE THE NEEDED DATA

Few product development companies have the comprehensive set of rules that IC manufacturers possess. However, they can still achieve the same opportunity to incorporate their DFX rules and best practices. The lack of a comprehensive and robust integrated software system can be supplemented by effectively organizing multifunctional teams of experts from each function. The knowledge needed to define the design and development requirements is provided by the experts from each function. This "manual" approach is providing quantum levels of improvements over

traditional design methodologies in many companies and for limitless product types.

This approach often is very effective because the individual engineers representing all the functions have the opportunity to be innovative and create better solutions when addressing the issues. The manufacturing engineers also know of the new processes and technologies that must be considered when introducing new products. Only the individuals responsible for the specific processes within the company or the key suppliers know all the metrics, the limitations, and the characteristics to expect when the product is to be manufactured. The multifunctional team that uses the DFX tools, resources, and technologies available can be very effective.

Many examples exist where new product development teams have reengineered their development processes to incorporate the right organization, processes and apply DFX criteria. The results demonstrate developing products in thirty to fifty percent of the time previously required. Substantial improvements are gained in the cost, performance, quality, responsiveness, and flexibility of the resulting manufacturing process. The results provide more revenue, profit, and market share. These benefits are essential to short and long term success.

REENGINEERING, MORE THAN A FAD

Pay Attention to This Buzzword. Reengineering is like many other concepts. Many, many people were doing it before they knew what "It" was. The process could be called "doing the right things" or "that is how we operate." Like so many things today, unfortunately buzzwords and acronyms rather than internal proposals capture the attention of so many executives. It often fits into the "silver bullet" or "add water and stir" approach to solving America's management problems. However, this is one technique to pay attention to and not ignore. This is one methodology that will facilitate major change in a very short time. It provides a very effective way to develop and optimize the most effective product development process for a company. Fortunately it is quite easy to implement and use.

Reengineering can be very easily applied by the smallest of organizations. Typical product development Core Teams have less than ten members. Often, that is the size of the entire engineering department or company in a smaller company. The potential benefit is especially important for smaller companies that do not have processes documented or well thought out. The process forces people to completely think about the total process rather than optimizing each separate function. It develops the most effective alternatives to develop products in much less time. This is accomplished while people representing the entire development, manufacturing, and distribution process are present to insure that all objectives are met.

This also applies to the largest of companies. Few companies have taken the time to optimize their development processes. If they have documented them, it is doubtful that the documentation is current and will not likely represent the processes that will be in existence when the new products are introduced. This is because many companies are actively pursuing a continuous improvement approach to manufacturing and are continually improving the manufacturing processes.

The only people that really know what is currently happening in a manufacturing operation are the people working there. The people that know the processes are the Process Engineers, Manufacturing, Tooling, Test, Quality, and other engineers; the managers, the suppliers and the people working in the processes. They know what and when process improvements should be made. This is the real knowledge database that exists in most companies and it is essential that these people be the ones that are involved in the reengineering process. They know the exact details of every desirable DFX issue and know how and when they can and should be used. The entire process can be developed and analyzed at the same time and optimized for maximum effectiveness.

There are equivalent resource pools in the other functional areas. Key people from Engineering, Sales, Marketing, Quality, Materials, Management, Cost Accounting, Suppliers, Regulatory and others are ready and willing to participate in finding ways to develop competitive advantages and compelling products. They have the ball and the game cannot be played without their direct involvement. These people must be directly involved. They have the knowledge and abilities to make the best decisions. This means that some outside person can develop better plans than they can do themselves. It simply does not make sense.

The resulting reengineered process is the composite of all the good ideas, DFX tools, innovative ideas, best practices and best judgements of the people involved in the product development and the process owners. It also provides a format to include the best ideas of key Suppliers and key Customers. It provides a mechanism to achieve agreement between the Development Team and Management regarding the objectives, the processes, the investments, and time frame to achieve the objectives.

REQUIREMENTS FOR EFFECTIVE DEVELOPMENT TEAMS

The importance of multifunctional development teams is accentuated because the process relies upon the internal knowledge, expertise, judgment, innovation and other capabilities of the specific individuals involved in the reengineering project. The Framework for information described in Figure 3 is typically not available and must be provided by direct interaction between the individual team members. The functional departments must be represented

either on the Core Team or Extended Team. Co-location of the Core Team is also very important for all the reasons described in articles regarding effective product development organizations.

DEVELOPMENT TEAM MEMBERS

The multifunctional team should be chosen and the Team Leader selected. This would include the Core and Extended team members. Each person would represent one key function required to successfully develop the product. The Team Leader is typically from R&D or Product Management but any qualified person could be the team leader. This person is the key contact point with Senior Management and provides the leadership, coordination, and control of the project for the team. It is better to have this person monitor and manage performance to the resulting schedule. It is strongly recommended to not have a "project coordinator" specifically for the purpose of managing the project and schedule as will be explained later.

The functions represented on the teams depend upon the specific product to be developed. The following functions would be represented for a typical product with electronics, firmware or software and some mechanical features other than packaging of the product. This is not a rigid recommendation and individual teams may suggest more or fewer functions represented on the Core Team. Some teams may only have three or four total members.

<u>Core Team</u>	<u>Extended Team</u>
Team Leader	Sales
Circuit Design	Human Resources
Mechanical Design	Management
Test Engineering	Key Suppliers
Manufacturing	Service
Quality	Key Customers
Software/Firmware	Reliability
Procurement	Cost Accounting

The team members are expected to represent their function on the team and can speak and commit for their function without always going back to the "boss" for a decision. The tasks and times to accomplish each task must be agreed to by each of the individuals on the team. This requires that the representatives be well-qualified members of the departments they represent and able to make decisions without undue double checking with their manager. It requires that the team members be qualified to make decisions that their managers agree to and will support. Their managers will be aware of the decisions that must be made and when the decisions are due. The comprehensive schedule that will result from this process requires that the functional management review, agree or modify, support and commit to the resulting reengineered process and schedule. The team members and their direct managers will be aware of the nature of decisions and commitments that must be made well in

advance of the date required. They will have adequate time to plan, decide, and commit to the decisions.

PREPARATION TO REENGINEER THE DEVELOPMENT PROCESS

Specific objectives for the product or product must be clear, understood and agreed upon by all Functional Managers, key individuals and the team members. This considers the Business, Marketing, R&D, Manufacturing, Sales, Financial and other key objectives. Reengineering the product development process should focus on a specific product or product family. Reengineered processes for a specific product can be easily expanded to a family of products or a product line. It is very important that the specifications of the product be agreed upon by all parties before starting the design of the particular hardware and software. This does not preclude the use of reengineering a process to determine and define the specifications. However, it is very important that the specifications be firm and agreed to by all parties; especially Sales, Marketing, and R&D, before detailed hardware design is begun.

It is particularly important that the departments have agreement upon which specific DFX criteria they want incorporated into the reengineered process. It is also important that each set of criteria be documented and understood so that all team members can help modify or support to result in a better product. For example, if Design for Serviceability is considered, there should be objectives and an appropriate set of actions, results, and metrics to support the requirement. The Design for In Circuit Test has a specific set of criteria that is dependent upon the devices used, the placement equipment, the test equipment, and the techniques to test and analyze the circuits, electronic assemblies, and final products. These techniques and requirements are usually well understood and documented.

REENGINEERING THE DEVELOPMENT PROCESS

The team members develop complete lists of the tasks and expectations required to design, develop, manufacture, test, and package the product. This list should be developed by the team member and the other key people in the functional department they represent. Considerable thought should be invested to develop the products expecting that there will be no engineering changes required. It should also be expected to arrive at a product that has the lowest cost, highest performance and quality. This may sound unreasonable but these conflicting requirements can be usually met with the ingenuity and creativity of the individuals and still introduce the products in much less time.

The full team will develop a Process Map of the processes and procedures to develop the product that meets all the objectives and incorporates all the DFX and other tools and best practices. This resulting process represents the integrated model of the most effective process to develop the product. It will include all the milestones, tests, reviews, and

requirements defined to develop products. The resulting logic of the individual tasks in the Process Map is reviewed, modified, improved and worked with until all parties agree upon the results.

The resulting map is typically a very complex item. The team needs a tool to work with this map to optimize, manage, and complete. Project Management software for PC's is ideal. The map is entered as a PERT Chart and then all the power of project management software can be applied to the map. The process map incorporates all the development objectives, milestones, reviews, tasks, activities and DFX tools. It insures the best possible product is developed in the least time without abusing people or short cutting the standards, specifications, or objectives.

Project Management software, such as Microsoft Project, provides a powerful tool set to optimize the result. Special reports for the Team Leader, each individual team member and management status reports are readily available. This software has almost too much capability. The recommendation is to only use the basic capabilities. Avoid trying extra fancy or complex features until people are experienced in managing projects with the basics. After the plan is complete, it is suggested the team work with and record progress and status on hard copy paper reports and avoid working in the computer. Experience suggests that as much time can be spent keeping the computer updated as is required to develop the project.

APPROVAL OF THE FINAL PROCESS AND SCHEDULE

The final development schedule should be reviewed and approved by the total team. The result should be tested against all the project objectives. Project Management software provides immediate projected dates for completion. In depth critical path analysis should be conducted to thoroughly review the logic, reality, and robustness of the final schedule. The final result is then reviewed by Senior Managers and approved. Special attention should be focused to insure that all the elements of the DFX criteria are effectively and efficiently satisfied. The final approval of the schedule is essential before beginning development. Beginning major design and development before the Development Team and managers agree is a poor practice and often causes problems later in the project because of misunderstandings at the beginning.

The management approval to begin starts the actual and formal development process. Regular weekly status meetings, held on Monday or Tuesday of each week are essential. Special care should be taken to avoid long, inefficient, and boring meetings. Conduct quick status meeting and let everyone get back to work. Anyone experiencing problems meeting their commitment should advise the Team Leader and work out the details before they become late. Every

effort is to meet the dates on or before the task is due and micromanaging is absolutely to be avoided. Team members are responsible for their own independent professional work and the Team Leader is not expected to provide regular encouragement to meet dates or performance criteria. That is the responsibility of the individuals.

MANAGING TO SUCCESSFUL COMPLETION

The Development Team is involved until the project is managed to successful completion. This means meeting or exceeding all the expectations. It also involves learning from the process about refining estimates, avoiding weak components, choosing stronger suppliers, focusing on critical issues, etc. These new lessons learned and best practices should be incorporated into the basic development process and considered for inclusion into the next project.

Regular management reviews are typically included in all development processes. They are also included in the reengineered process. The frequency and timing is negotiated with the appropriate managers. This can also sometimes include key customers. Care must be taken to remember that Senior Managers are a very important group of Customers. Key managers, like key customers, are very important and need to have good communications. This does not mean that specifications should be allowed to change but managers do have a great deal of accountability and responsibility to the company. They must be informed and aware of the status of the company's investments in new products.

TYPICAL RESULTS

The typical results from a large number of reengineering projects are truly impressive. These are some common results achieved for reengineered product development processes:

40-70% Reduction in Product Development Times
15-40% Reduction in Product Costs
40-80% Reduction in Number of Parts
40-90% Reduction in Product Assembly Times
30-90% Reduction in Manufacturing Lead Times
50-80% Reduction in Manufacturing Space
25-65% Reduction in Number of Suppliers
15-70% Reduction in Tooling Costs
25-90% Reduction in Engineering Change Orders

CONCLUSIONS

The Product Development Processes are the most important processes within any company. Very strong growth in the global electronics market and tremendous competitive pressures will significantly increase the demand to develop more competitive products in significantly less time. The processes are affected by nearly every functional department from Sales through Distribution and Field Support and every function has a meaningful input into how to best design and develop the product. The total process should be reengineered by the people on the development team. The Product Development Process includes tasks, reviews, milestones and DFX issues that satisfy the requirement from each function to produce the most competitive product possible. Each person on the team has the opportunity to define their tasks and time required to complete the tasks. It typically requires a Development Team about ten days to reengineer and develop a comprehensive plan and schedule. The resulting plan produces specific tools for each individual that defines what and when their tasks need to be completed. Design for X rules, principles and guidelines must be considered at the very beginning of the development process to most effectively impact the final result. Major improvements in competitiveness are gained by effectively addressing the development process and using DFX principles.

ACKNOWLEDGMENTS

The author would like to thank Mr. Happy Holden of the Hewlett-Packard Company for his ever present challenges and motivation to find more effective product development processes.

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DESIGN FOR FABRICATION

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INTRODUCTION

The focus of this paper is on Design for Manufacturability (DFM) from the bare board fabricators' perspective. In the mid 1980's the PWB (Printed Wiring Board) industry began to feel the impact of the increasing complexity of integrated circuit packaging. Since then we have seen the transition from 16 pin dual in-line packages with leads on 0.100 inch centers to 340 pin ultra fine 0.012 inch pitch components. To compound matters, the density of the components increased as the number of functions required per board increased. Initially, the term "manufacturability" referred to the capabilities of insertion and placement equipment i.e. component orientations, spacing, heights, etc. In an effort to improve yields, bare board manufacturers began to follow the lead of the assemblers who had already initiated Design for Assembly (DFA) programs. By 1987 several large captive manufacturers had developed formal approaches to DFM and were actively working with their PWB designers to improve manufacturing yields. Some of the obvious benefits of designing manufacturability into bare boards include:

- Higher quality
- Reduced lead times
- Lower labor and material costs
- Higher first pass yields

Because of the success of these early DFM programs, they have become an integral part of the preproduction engineering departments of many North American fabricators.

The evolution of these DFM programs during the last decade can be broken into three distinct phases:

- Establishing the DFM discipline
- Automating the DFM analysis
- Expanding the DFM scope

The first phase of these programs was the domain of the fabricators. Using traditional methods and technology preproduction engineering departments developed screening methods to manage the increasingly complex designs that resulted from surface mount technology. As the discipline matured and the benefits of DFM were established, third party tooling software suppliers recognized the need for greater analytical speed and accuracy thus initiating the second phase.

Today we have entered a new phase with the advent of automated repair software. This software allows for rapid, reliable "repair" of design problems that are detected in the analysis.

ESTABLISHING THE DFM DISCIPLINE

The DFM programs developed by fabricators have rating methods for assessing manufacturability or producability of a given design. These scoring schemes, whether manual or highly automated, take into consideration three critical factors:

- 1) Component packaging technology and associated design attributes i.e. hole sizes, annular rings, traces and spaces, etc.
- 2) Complexity factors which characterize the complexity of the design attributes
- 3) Manufacturing cost drivers

1) Component Packaging Classes and Associated Design Attributes

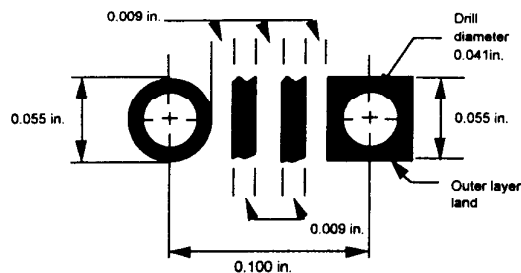
The choice of component packaging technology determines the requirements for hole sizes and tolerances, traces and spaces and many other critical design factors which impact the manufacturing yields. Therefore, the first step in setting up a DFM rating scheme is to categorize designs from least complex to most complex based on component packaging technology. A design with 16 pin DIP packages would represent the least complex while a design incorporating 340 pin ultra fine 0.012 inch pitch components would represent the most complex.

Class	COMPONENT PACKAGING
I	<i>Low density:</i> Through hole designs (one or two traces between integrated circuit pins placed on 0.100 inch grid).
II	<i>Medium density:</i> Typically mixed through hole and surface mount technology designs (one trace between vias placed on 0.050 inch grid).
III	<i>High density:</i> Surface mount designs, two and three tracks between feed through holes placed on 0.050 inch grid.

Table 1: Component Packaging Classes

The second step in developing a rating system is to determine what are the typical physical characteristics associated with the design classes. This is relatively simple as the CAD (Computer Aided Design) systems require pad geometries in order to set up the component libraries. The pad geometries in turn determine the largest size trace which can be used to provide connectivity when the design is routed. The size of any required component or feed through holes is also fixed by the pad geometries.

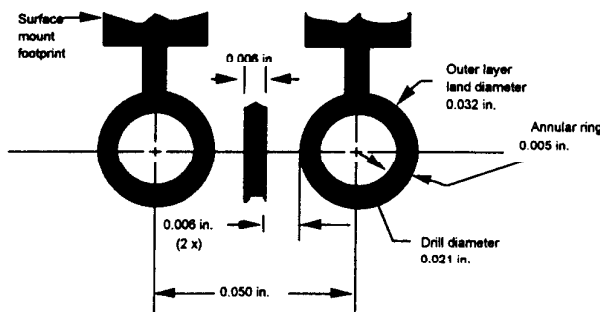
Figure 1 is an example of pad constructions for a 16 pin DIP package. This design has two traces routed through 0.100 inch centered through holes (in the illustration above, this design would be a Class 1, low density design):



- Pad diameter 0.055 inch
- Hole callout $0.035 + 0.005/-0.005$ inch; preferred drill diameter 0.041 inch
- Trace width 0.009 inch/space width 0.009 inch

Figure 1

The following is an example of preferred pad constructions for a surface mount design which has one trace through 0.050 inch centered via (feed through) holes (in the illustration above this design would be a Class 2, medium density design) :



- Pad diameter 0.031 inch
- Hole callout $0.021 + 0.000/-0.021$ inch; preferred drill diameter 0.021 inch
- Trace width 0.006 inch/space width 0.006 inch

Figure 2

Understanding the design attributes required by the selected component packaging technology allows one to set up subcategories for each design attribute. From a bare board

perspective, the component packaging technology is commonly referred to as "6 and 6", "5 and 5", "4 and 4", etc. referring to the traces and spaces required in the routing of the different design densities.

The third step is establishing a scoring methodology which results in a numerical rating. Appendix I shows an example of a matrix of attributes which have been associated with given component technologies. A Complexity Index or Matrix characterizing the complexity of physical characteristics (size, layers, holes, traces, etc.) allows one to easily calculate the first pass yield which is essential to both costing and pricing. Metrics establish a common language that links manufacturing to design. The equations or tables allow for analysis of various factors and result in a numerical score. If the score meets producability requirements, then the design may be approved for tool and build. The following chart is an example of how the Hewlett-Packard Loveland facility has characterized first pass yield as it relates to increasing complexity.

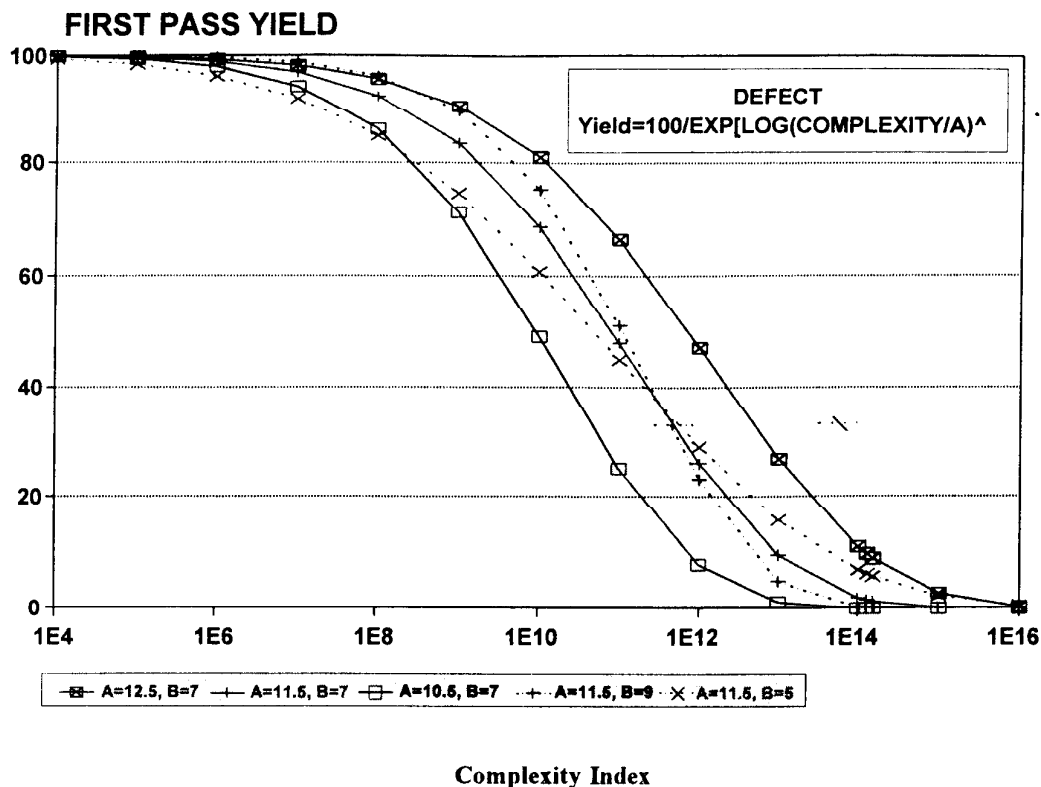
The fabricator's success depends on being able to characterize his processes and keep them in statistical control. The fabricator must understand processing variables or the ratings are meaningless. Process Engineering must design experiments (DOE) which characterize process capability with respect to the end product parameters. Several approaches have been taken to come up with manufacturing capabilities. DOE's may be run looking at a single attribute such as minimum drill capability, smallest trace and space on a given copper weight, etc. Another approach which has been taken is to select a representative design and systematically vary the design attributes to determine tradeoffs. Statistical process control must be in place in order for the stated capabilities to have any validity.

Understanding the design attributes required by the component packaging technologies combined with stated manufacturing capabilities allows the fabricator to develop "preferred pad constructions" as well as design rules and guidelines for optimum yields. For example, with reference to the pad construction shown in Figure 2 above, it would not be unusual to see an 0.008 inch trace, 0.008 inch spaces and correspondingly smaller drill diameters and pad sizes. However, depending on the thickness of the board, the resulting aspect ratio could present problems for the fabricator. *The goal is to simplify the product and make it easier and less costly to manufacture.*

2) Complexity Factors

The following are typical design attributes which can be physically measured, associated with one or more component technologies and represent varying degrees of difficulty in the manufacturing process:

- Inner and Outer layer trace and space width
- Drill diameters/Finished plated hole tolerance



- Annular ring
- Clearance pad diameters
- Nominal finished board thickness
- Board thickness/hole size/aspect ratio
- Copper clad weight of the laminates/foils
- Overall finished profile tolerance

It should be noted that although the attributes are common to PWB's, manufacturing capabilities are vendor specific. The IPC (The Institute for Interconnect and Packaging Electronic Circuits) has recognized the need for vendor qualification, and has introduced a document aimed at assisting OEMs in evaluating and assessing the capabilities of PWB fabricators, IPC-1710, "Manufacturer's Qualification Profile."

The following is a brief discussion of the key design attributes and how they impact bare board manufacturer:

1) Minimum Trace and Space Width (typically measured on the master plotted artwork).

The smaller the line width, the more challenging the image reproduction as it relates to imaging and etching. The designer must understand the fabricator's line width capabilities and the expected yields. The thickness of the copper is a key factor for achieving minimum line width within required tolerances on outer layers because of the

additional pattern plate. The minimum line width improves significantly with 0.5 oz. copper clad in the 0.006 to 0.007 inch range and becomes a requirement in the 0.006 to 0.005 inch trace width range. This is especially critical to the designer who is working with impedance lines on the outer layers. It can be an unpleasant surprise to learn that in order to manufacture the design to specified impedance values the line widths must be reduced to 0.005 inch, but the outer layers were designed with 1 ounce material compromising the manufacturing yields and associated costs.

2) Minimum Drill Diameter

Fabricators' drilling capabilities are typically stated as the smallest drill size that can be used in a production mode. Stack heights (how many panels may be drilled at a given time) are determined in large part by the smallest drill size and can therefore, have a significant impact on the cost associated with drilling. The designer must be aware of their vendor's minimum drill size capability and what the associated cost is when selecting a technology set to ensure there is a good match. Minimum drill size is not only a driver for drilling cost, it may also have a significant impact on the reliability of the board as it impacts annular rings and aspect ratio (see below).

3) Inner and Outer Layer Annular Ring (The difference between the drill diameter and the corresponding circuitry pad diameter as measured on the master artwork.)

It is important that the designer not only understand the finished board specification with respect to annular ring, but additionally what the capability of the vendor is to meet this requirement. The pad constructions that the design has dictated must allow enough registration tolerance in order to fabricate the boards to customer specification. The fabricator may or may not include the plating in the hole wall (typically 0.001 inch of copper) when stating their capability. Issues with annular ring can often be resolved by increasing the pad size or decreasing the drill size.

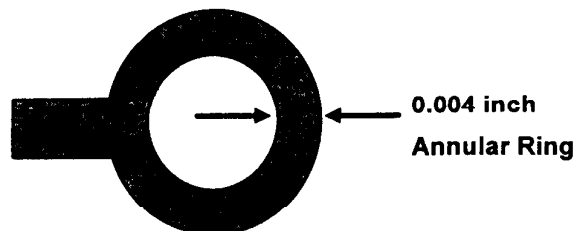


Figure 3

4) Ground Plane Clearance

Ground Plane Clearance refers to the removed portions of a ground plane that isolate it from a drilled hole in the base material to which the plane is attached. Clearance is determined by measuring from metal to metal on the master artwork.

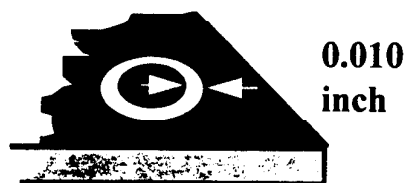


Figure 4

To ensure the minimum required clearance can be maintained on the finished board, the minimum required electrical clearance plus the image and drilling tolerances must be added together to determine the appropriate clearance pad diameter. (Refer to IPC-D-275 Design Standard for Rigid Multilayer Printed Boards and Rigid Printed Board Assemblies for specifics).

If the plane layer design leaves strips of copper between clearance pads, a minimum spacing must be maintained between clearance pads to avoid causing shorts due to resist lifting and redepositing. (Again measurements are taken on the master plotted artwork.)

5) Aspect Ratio

The *maximum* board thickness divided by the *smallest* selected drill diameter. The maximum board thickness is the calculated thickness over copper before plating. Additional thickness caused by plating, hot air solder leveling, or soldermask has no impact on aspect ratio.

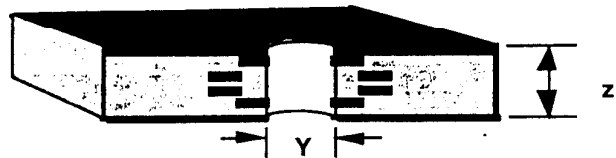


Figure 5

Aspect ratio is critical to reliable copper plating thickness in the hole wall. The greater the aspect ratio the more difficult the board is to plate and at some point the fabricator's ability to produce reliable product is compromised.

3) Cost Drivers

In addition to understanding how the design drives costs, the designer must understand the key cost drivers relative to bare board manufacture. The cost drivers are:

- Raw laminate - both panel utilization and material selection, i.e. mixed dielectrics, non-standard materials, etc
- Number of layers
- Number of different drill sizes and total number of holes
- Gold requirements
- Mechanical tolerances, i.e. plate thickness, hole-to-hole, edge-to-edge dimensions, etc
- Solder mask requirements
- Electrical test parameters
- Yield

When all factors are considered, complexity factors as well as the additional cost drivers, a "score card" can be developed to quickly and accurately predict first pass yields as well as price. The Table 1 below is an example of a score card approach.

In the late 1980's the first step in the DFM analysis was manually filling out a check sheet. The single image plots were measured and trace and space widths as well as pad sizes were recorded. Drill sizes were selected and manual calculations were made to determine the annular rings and aspect ratio for the design. This inspection step took several hours and was prone to errors. Design Rule Checks (DRC's) are generally a standard Computer Aided Design (CAD) system feature. However, they do not provide an adequate tool for assessing whether or not the design can be fabricated efficiently and at a reasonable cost. They do not take into account drill information that impacts two very critical variables in PWB manufacture, annular ring and aspect ratio.

The original intent of the Merix Complexity Factor Matrix and accompanying documentation was to aid the preproduction engineering department in screening jobs for producibility before loading new designs to the manufacturing floor thereby improving yields. It soon became evident that it would be beneficial to develop a

FABRICATION FACTORS	pts.	Highest	pts.	High Middle	pts.	LowMiddle	pts.	Lowest
Material of Construction	147	Polyimide	88	Cyanate Ester	49	FR-4	40	CEM III
Number of Layers	196	8 layers	137	6 layers	89	4 layers	36	2 sided
Number of Holes / Panel	270	<20,000	180	10,000 - 20,000	90	3001 - 10,000	27	1 - 3000
Lithography (traces & spaces)	25	> 4 mils	10	4 - 5 mils	6	6 - 8 mils	1	< 8 mils
Gold Tabs	48	3 Side, <4sq.inch or 2 Side, < 3.5 sq.inch.	32	2 Side, <3sq.inch or 1 Side, < 2.5 sq.inch.	16	1 Side & < 1.5 sq.inch.	0	None
Annular Ring	30	> 2 mils	21	2 - 4 mils	7	4 - 6 mils	1	< 6 mils
Solder Mask	25	2 Sided Dry Film	17	2 Sided LPI	10	1 Sided LPI	5	Screened - 1 side
Metalization	75	Electroplated / Reflowed Tin-lead	69	SMOBC / SSC	46	SMOBC / Electroless Ni/Au	29	SMOBC / Organic Coated
Minimum Hole Size	168	> 8 mils	84	8 - 12 mils	69	13 - 20 mils	5	< 20 mils
Controlled Impedance	105	+/- 5 %	62	+/- 10 %	30	+/- 20 %	0	None

Points are PER PANEL

For board, divide by # per panel

Table 1: PWB Score Card (Courtesy Hewlett-Packard)

DFM manual with rules and guidelines that could be used to train PWB designers. Some of the pitfalls could then be avoided at the design stage or worst case, soften the blow when manufacturability issues were encountered. The first edition of the Merix DFM manual went to press in June 1988 and has seen many revisions over the years.

Phase I of the DFM program evolution drew to a close with a solid foundation in place. However, the procedures for analysis were manual and cumbersome. Because artwork was required, problem detection was not quick enough to avoid wasted time and energy.

AUTOMATING THE DFM ANALYSIS

Fortunately, Infinite Graphics Inc. (IGI), a tooling software supplier, recognized the need for an automated design analysis. IGI software developers used the Merix Complexity Factor Matrix as a backbone and developed the SeriCAM PAR® (Producability Analysis Report) program. This pioneering program automatically reads the customer's design data and provides a complete design analysis. If there are potential tooling or manufacturing issues, communication can occur within hours rather than days.

Integrating an automated DFM program on the front end of the tooling stream significantly increases the output of a

tooling department. Merix, as well as many other PCB manufacturers, integrated PAR® on all incoming designs. This necessitated restructuring computer aided tooling (CAT) departments as well as converting preproduction engineering personnel from personal computers to X terminals. Tooling technicians were "transferred" to sales support teams.

Immediately upon receiving the customer data over modem or the Internet, the data is read into the tooling system. The drawings are plotted first so that the preproduction engineering activities as well as the DFM analysis can be run in parallel. Any custom apertures are set up and customer specifications are reviewed for any nonstandard requirements. The DFM analysis requires input of the design's hole size callouts including specified tolerances and plating type from the fab drawing. Merix tooling software support engineers developed an automated drill selection program that consistently and rapidly selects the correct drill sizes. After the drill sizes are assigned, the DFM analysis is run. Within an hour or two, this analysis can be reviewed by preproduction engineering. Any conditions that do not meet DFM requirements are resolved with the customer before loading the job to tooling. If single image artwork plots are required by the customer, they can be plotted in parallel with the analysis.

The software produces detailed reports, in both graphic and text formats, that list typical spacing values and deviations from desired specifications, soldermask values, surface mount pad geometries and drill summaries. The following detailed checks are performed:

Signal layer checks:

- Pad to trace spacing
- Trace to trace spacing
- Hole to circuit spacing
- Circuit to non-circuit spacing
- Trace Width
- Annular ring
- Geometry to board edge.

Plane layer checks:

- Clearance to clearance spacing
- Clearance annular ring
- Thermal annular ring

Soldermask Layer checks:

- Minimum trace overhand
- Minimum sliver
- Annular ring with signal layer

Solderpaste Layer checks:

- Minimum sliver
- Annular ring with signal layer

Silkscreen layer checks:

- Minimum line width

Ideally, the data generated by the DFM analysis is integrated with a traveler (manufacturing routing) generation system to ensure the appropriate manufacturing processes are selected. Merix has a sophisticated Computer On-line Tracking (COLT) system that drives traveler generation and the shop floor control system from a central database. The data generated by the DFM analysis is input into a part specific database.

An example of design characteristics that can be directly associated with manufacturing constraints are trace width and copper weight at the outer layer etch operation. If a design has 6-mil traces and spaces on the outer layers, a program can be written to ensure that the appropriate clad weight is selected (less than one ounce). A heavier clad weight may compromise the trace width at outer layer etch after plating. It is also more cost effective as well as environmentally friendly to use the lighter clad weight. A second example of how a design characteristic drives manufacturing processes is with respect to parts with high aspect ratios. The diameter of the minimum drill as well as the calculated thickness of the board after lamination can be used by the system to determine aspect ratio. An algorithm can be run to determine what type of copper plating the hole wall will receive based

upon the calculated aspect ratio. If high aspect ratio plating programs are called for, preproduction engineering can be flagged on-line and any necessary adjustments to trace widths in order to meet specified impedance requirements can be made. Because of these types of sophisticated algorithms, Merix first pass yields on impedance boards is very predictable.

Manufacturability issues not so easily quantified and for which manufacturing capabilities have not been characterized remain problematic. These "gray areas" are more difficult to automate and thereby simplify. Without metrics, establishing rules and guidelines are difficult. Internal low pressure areas and plating imbalance result from designs that do not have "good" circuitry distribution. Product Engineers are routinely relied upon to troubleshoot these types of manufacturability issues. Guidelines and suggestions rather than rules are typically the norm.

For example, the Merix DFM manual states, "Circuitry area and distribution between front and back of the board should be balanced within 10%. Plating thieving of low pattern density and cross hatching of external plane areas should be considered." Process characterization studies need to be performed to determine where yields are impacted before our tooling software partners can supply the solutions for automated DFM checks as well as repair.

The overall benefit of an automated design check is a significant reduction in cycle time for customers as well as improved accuracy. Some side benefits have resulted as well. Single image plots are no longer needed in order to "view" the board design. The data can be viewed in the X-terminal graphical window environment. Critical line width measurements can be made on-line more quickly and accurately than waiting for single image plots to measure with a microscope with a measuring reticule. Automated Optical Inspection (AOI) of the photo tools as a means of checking for spacing violations becomes unnecessary.

Due to the difficulty of maintaining controlled hard copy issues of DFM manuals converting to an on-line system may prove beneficial. The hard copy manual can be replaced with computer disks so that customers can also put the information on-line for use on their systems. In the past large design centers received as many as twenty hard copies that quickly became outdated. Today an updated disk can be delivered periodically to a customer focal point and the information updated on-line. The plan for the future is to put the Merix DFM information on the World Wide Web allowing Product Engineering to provide real time updates.

Documentation and CAD Data Check List

These are the minimum requirements necessary to perform a manufacturability assessment:

- CAD Image data (Gerber Data or IPC-D-350)

- Aperture lists
- Drill files (X,Y coordinates)
- Fab (mechanical) drawings (HPGL files)
- Net List

Preferably this data is transferred via a modem or the Internet.

PHASE III: EXPANDING THE DFM SCOPE

An area that still presents opportunities for both tooling and manufacturing is related to problems with the dimensions on fab drawings. Often dimensions are missing or incorrect. The tolerances may leave no latitude for drilling or profiling. If the customer provides a board outline with the CAD data that is to scale, this outline can be checked to the fab drawing. It may also be used later in the panelization process as well as in developing the NC profile program. If a usable board outline is unavailable, a board outline must be created much earlier in the tooling process. This step will again move resources from the traditional CAT role back up into the processes, eliminating redundant steps and catching errors closer to the source before value is added.

The next major step in the development of DFM software is "DFM based automatic editing". Editing on tooling workstations is inefficient, time consuming and subject to error at best. When the DFM analysis identifies a "design error" the question becomes who edits the CAD data and who updates the customer CAD files? This is particularly difficult when the problem has no impact on the performance characteristics of the design, but is a problem for fabrication. Merix is currently evaluating software that will increase the manual editing speed and quality. On-line design rule and netlist checks that are tied to materials and stackup information via a unified open database will prevent introducing new violations during the manual edit sessions. This will maintain both design integrity and manufacturing optimization. Chuck Feingold, Valor Computerized Systems, describes this next step forward as making the DFM programs "three dimensional" by adding the board construction as well as the functionality to the analysis. Knowing the design will not be compromised by manual edits, allows fabricators much more flexibility in "modifying" the CAD data to improve manufacturing yields.

A second new technology that will revolutionize DFM programs is Product Data Management (PDM). Today, it is the fastest growing technology within the scope of "CIM (Computer Integrated Manufacturing) related investments. According to CIM data's Product Data Management Technology Guide, "PDM provides a means to manage all product related information as well as the processes utilized throughout the product's entire life cycle. PDM integrates and manages processes, applications, and information that define products across multiple systems and media." PDM

systems and methods provide a structure in which all types of information used to define, manufacture, and support products are stored, managed, and controlled. Typically, PDM will be used to work with digital files and database records. These may include:

- Specifications
- CAD drawings
- Geometric models
- Images (scanned drawings, photographs, etc.)
- Engineering analysis models and results
- Manufacturing process plans and routings
- NC part programs
- Electronically stored documents, notes, and correspondence
- Hardcopy (paper-based) documents (by reference)

In short, any information needed throughout an interconnect product's life can be managed by a system, that makes correct data accessible to all people and systems that have a need to use them. This will allow both product and process engineers to view the customer data and all appropriate tooling files. Annotations can be made by a product engineer for reference by anyone needing to view the data. One of the successful PDM installations specific to our industry has been the Star 1000 Engineering Information and Archiving system. Companies using this technology report much reduced interruptions of their tooling resources.

CONCLUSION

The same benefits that were achieved when DFM programs were first implemented in the late '80's can be achieved more quickly and reliably today with automated DFM checks and repairs. Design for Manufacturability programs are evolving from manual design rule checks (enhanced by the addition of the fabricators drill information and material stackups) to on-line design rule and net list checks. Next generation preproduction, engineering systems are becoming available, that are based on open file formats and object oriented programming.

In reviewing the literature, the common theme for both Design for Assembly and Design for Fabrication is that the analysis is "too often postponed until after the design has been completed and the product is released to the fabricator and/or assembler" resulting in unnecessary delays and expenses. The analysis is too late in the design process to have maximum impact. The New Product Introduction (NPI) process is all one direction, from Design to Manufacturing. Because of this "one way" flow of information, fabricators and assemblers have developed DFX (Design for Assembly/Manufacturing) programs to protect their manufacturing operations from designs which negatively impact yields or disrupt the manufacturing process flow. Fabricators have developed DFM manuals and training

programs for their customers in an effort to minimize the number of designs which must be redesigned in order to be manufactured in a competitive manner. The current state of the manufacturability assessment may best be described as "Redesign for Manufacturability."

ACKNOWLEDGEMENTS

The author would like to thank the following individuals for their input to this article: Chuck Feingold, Valor Computerized Systems, Happy Holden, Hewlett Packard Co. and Cliff Stritch, Infinite Graphics Inc.

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APPENDIX

COMPLEXITY FACTORS MATRIX (June 1995)

CATEGORY	INN	DRI	LAM	OUT	PLA	SM	FIN	DIMENSIONS
Trace Width		1 2 3 4		1 2 3 4		3 4		GE 0.007 GE 0.005 & LT 0.007 GE 0.003 & LE 0.004 LT 0.003
Space Width		1 2 3		1 2 3		3 4		GE 0.007 GE 0.005 & LT 0.007 GE 0.003 & LE 0.004 LT 0.003
Annular Ring Radius	1 2 3 4	1 2 3 4	1 2 3 4	1 2 3 4				GE 0.0085 GE 0.0065 & LT 0.0085 GE 0.004 & LT 0.0065 LT 0.004
Clearance Pad Radius	1 2 3 4	1 2 3 4						GT 0.0085 GE 0.018 GE 0.010 & LT 0.01375 LT 0.010
Overall Profile Tolerance							1 2 3 4	GT ± 0.008 GT ± 0.004 & LT ± 0.008 EQ ± 0.004 LT ± 0.004
Finished Hole Tolerance					*			GE ± 0.003 Go-No

Key:

INN ----- Inner Layer

DRI ----- Drilling

LAM ----- ML Lamination

OUT ----- Outer Layer

PLA ----- Plating

SM ----- Solder Mask

FIN ----- Finishing (Profiling)

GT ----- Greater Than

GE ----- Greater than or Equal to

LT ----- Less Than

LE ----- Less than or Equal to

EQ ----- Equal to

Note: All dimensions are in inches

DESIGN FOR ASSEMBLY

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INTRODUCTION

Evaluating assembly efficiency of the surface mount product is too often postponed until after the design has been completed and the product is released to production. Design for Assembly efficiency is a process that should start during the products conception. With the cooperation of designers, manufacturing and test engineers, materials specialists and development engineers, most issues related to manufacturing efficiency can be resolved without impacting program schedules. The benefit of this concurrent activity during the products development phase ensures a smoother transition of the product into manufacturing. The term "Design for Manufacturing" (DFM) means more than efficient assembly... a product that is designed well should also be competitive in cost while providing a long and reliable service life.

Surface Mount assemblies, especially those with ball grid array, fine pitch and micro ball grid array devices, require continuous process monitoring and methodical inspection. For example, solder joint quality in the U.S. is generally measured against a criteria defined in both IPC-A-620 for overall workmanship and the National Solder Standard, ANSI/J-STD-001 which defines the requirements for a reliable solder connection. Understanding these guidelines and standards, the PC board designer can develop the land pattern geometry's that will provide the opportunity for process engineers to meet the industry established requirements.

MANUFACTURING EVALUATION

Design for Assembly (DFA) includes all aspects of the manufacturing process:

- o Design for Assembly
- o Design for Testability
- o Design for (PCB) Fabrication

Before releasing a new design to manufacturing for volume assembly, a DFA evaluation of the finished surface mount product should be performed. The evaluation will include a thorough review of documentation, CAD generated data, materials and finished hardware (and when available, a prototype assembly).

ASSEMBLY DOCUMENTATION REQUIREMENTS

The preparation of clear and complete assembly documentation is vital to the successful transition of the

product from the design/engineering environment into a production environment. Individuals developing the documentation and other necessary data for manufacturing should be aware of the expectations and requirements.

DOCUMENTATION AND CAD DATA CHECK LIST

- o Bill of Material (BOM)
- o Approved Vendor List (AVL)
- o Assembly Detail
- o Special Assembly Instructions
- o PCB Fabrication Detail
- o Gerber Data or IPC-D-350 File on Disk

CAD data is especially useful for developing machine tooling, programming of automated assembly systems as well as process and test fixture preparation.

DATA REQUIRED FOR ASSEMBLY PROCESSING

- o X-Y Device Coordinate Data
- o Testing Requirements
- o Schematic Diagram
- o Net List
- o X-Y Test Probe Locations

Although hard copy data is acceptable for X-Y coordinate and net list, CAD information supplied on disk media is preferred.

EVALUATING THE SMT PC BOARD QUALITY

A solder sample is selected from each board lot or specific date code. The circuit substrate is compared to the fabrication detail and specified IPC quality level established. Following physical inspection, solder paste is applied to the SMD land patterns of the sample. The non-populated substrate is processed to reflow the solder paste and if organic flux is used, aqueous cleaning typically removes residue. The reflow solder quality will be evaluated as well as the substrates physical reaction to the temperature cycles of the reflow systems. A similar test is performed using the wave solder process.

FINE PITCH AND uBGA TECHNOLOGY ISSUES

Fine Pitch and uBGA assembly represents an understandably advanced packaging and manufacturing concept. Component density and complexity is far greater than many commercial products and if assembled in high volume, several issues must be addressed before an automated process can be developed. For example, the Fine Pitch components having

a lead spacing of 0.65mm (.025") or less are adapted to both standard and custom application specific integrated circuits (ASIC). Industry standards for the Fine Pitch family of devices have extremely broad mechanical tolerance that must be considered when developing the land pattern geometry and spacing typical of that defined in Figure 1.

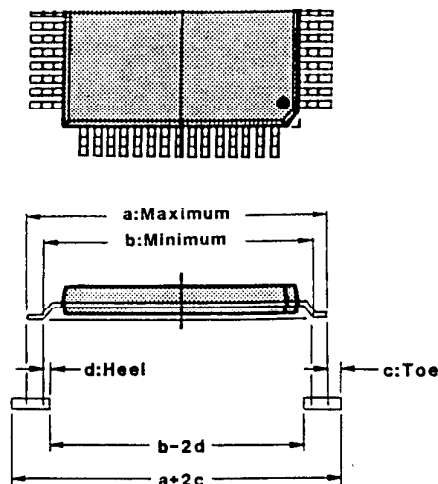


Figure 1. Land pattern geometry on Fine Pitch devices should allow for both Least Material Condition and Maximum Material Condition.

Because the tolerances will vary a great deal between suppliers and although one may mathematically develop a geometry suitable for attachment of the Fine Pitch device, land patterns must often be tailored or refined before efficient assembly process yields are achieved.

Ball Grid Array devices in comparison, are dimensioned without MMC/LMC factors associated with formed lead configurations.

The Ball Grid Array (BGA) and Micro Ball Grid Array (uBGA) family of products on the other hand have proved to be far more efficient as far as assembly process yield. Although the array devices are not as widely used as the fine pitch configuration at the time of this writing, the BGA and uBGA packages have closely defined physical attributes and uniform land pattern conventions.

USE PROVEN SMT LAND PATTERN GEOMETRY

Land pattern sizes and spacing generally follow recommendations furnished in IPC-SM-782A. Geometry of specific land patterns may deviate from those shown in the IPC document however, to meet specific process requirements. Land pattern length for wave solder processing for example, may be extended by an additional 2.5mm (.010") from the lead or contact end to provide exposure to flux and solder. Devices that are consistently supplied at

either extreme of the established tolerance limits (LMC or MMC) may also need an adjustment to recommended land pattern geometry's.

CONSISTENT ORIENTATION OF DEVICES

Although consistent orientation of devices on the PC Board is not mandatory, uniform direction of similar device types can improve assembly and inspection efficiency. For assemblies having mixed technology, leaded devices attached in a common orientation reduces assembly time because the placement head is generally in a fixed position and the board must be rotated. (surface mount assembly systems on the other hand, can rotate the devices before placement). Consistent SMT device orientation, although preferred, is not a factor for reflow solder processing but if the devices are attached using a wave solder process, device placement should be consistent and the direction of the device adjusted to maximize exposure to the wave.

POLARIZED DEVICES IN ONE DIRECTION

The direction of the polarized device, diodes, tantalum capacitors and even ICs, may be dictated by the function of the circuit. Process engineers recognize that performance of the circuit takes priority over assembly efficiency but, common polarity of device types or families adds to the overall producibility of the SMT assembly. When a common polarity or direction of device families can be achieved, machine programming is simplified and fewer errors will occur during assembly. In addition, visual or automated inspection is more efficient and overall process yield is generally better.

UNIFORM AND ADEQUATE DEVICE CLEARANCE

Automated surface mount device placement is very accurate but designers attempting to maximize component density may not be aware of all manufacturing complexities. In order to maximize process yield and assembly efficiency, recognize the requirements of specific soldering processes, inspection criteria and repair techniques. Tall components that are too close to a fine pitch device will restrict the angle of view needed to inspect the solder joint and access by rework or repair tools will also be hampered. Wave soldering is common for the lower profile chip devices, diodes and transistor packages and small outline IC (SO IC) devices can be wave soldered as well but some packages may not withstand direct exposure to the molten solder. To ensure consistent attachment quality, space between devices must allow for uniform exposure to the solder. To ensure that solder contacts all termination points on devices during wave soldering for example, taller components must be spaced away from the low profile device to prevent shadowing.

SMT DEVICES USE STANDARD CONFIGURATIONS

Standards have been developed by the national and international electronics industry associations for most

surface mount devices. When possible, select device packaging controlled by these standards. This will help the designer in maintaining a uniform land pattern library in the CAD system and process engineers will have more control over the assembly processes. The designer may find that standards for components have been developed in other countries and although similar in appearance, differ to a degree from devices developed domestically.

As an example, small outline devices supplied from European and North American companies meet EIA/JEDEC standards while Japanese manufacturers may adhere to EIAJ furnished specification. In selecting the device package from multinational suppliers use a degree of caution. Because of the somewhat liberal tolerances of the EIAJ standards, the designer cannot assume that the physical dimensions of the devices are consistent between one manufacturer and another.

Products submitted for standardization by the JEDEC members today must meet internationally recognized dimensioning guidelines. All components must be dimensioned using the metric system. Any device submitted for consideration in "inches" will be rejected. Because standards are developed using only metric factors, device packaging standards developed for fine pitch and ball grid array are far more uniform.

COMPONENT PARTS HAVE MULTIPLE SOURCES

Discrete passive and generic active devices are available from several sources. Although single source devices may be necessary for specialized functions, two or more suppliers should be qualified for other devices when possible. It is not uncommon for a company to select three alternative sources for devices and typically one or two are considered primary sources and a third as a backup. Having multiple sources will avoid the inconvenience of shortages due to the industries difficulty in forecasting supply and demand. Of equal significance to those attempting to control manufacturing costs, single sourcing does not allow any leverage for the buyer when negotiating price.

DESIGNED FOR EFFICIENT SMT PROCESSING

Assembly processing of the board can be relatively simple or, depending on the component types and density, more complex. The complex design however, can be efficient to manufacture and the less complex made difficult if the designer does not understand the requirements of each assembly process step. Assembly planning should take place during the preliminary phase of the design layout. Often, by adjustment of a components location or orientation and polarity direction on the PC board, manufacturability can be enhanced.

When the PC Board is small, irregular in shape or devices are very close to the board edge, panel array

recommendations can be considered for a uniform panel array format.

DESIGN FOR TEST AND REPAIR

The detection of assembly process or device defects with bench top analyzing equipment is time consuming and may add significant costs to the product. Whether manual or automated, a test strategy should be defined before the PC Board design is started. If the test method selected uses automated In-circuit Test (ICT) for example, probe access must be available at specific common connecting circuit points. Though most component malfunctions may be detected through in-circuit and diagnostic capability built into a functional test system, there is considerable concern that specific solder process defects will be difficult to identify.

Test systems can be programmed to automatically measure the function of each device on the completed assembly. The automated system can also detect and locate improperly placed or damaged components and identify solder process defects. Process defects include both bridging of solder between the leads of devices and open connections between the device lead and the board's land pattern.

The in-circuit test systems are fixtured and programmed specifically for each assembly type and when the board has been designed for testability the system will efficiently detect both component failure and assembly process (solder) defects. Figure 2 illustrates a solder bridge defect that may be identified with visual inspection however, insufficient solder or a very small alloy bridge on the fine pitch devices may escape detection unless electrical testing methods are employed.

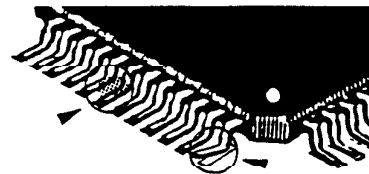


Figure 2. Solder defects may be detected visually however, in-circuit electrical test is a more reliable method of monitoring assembly process defects.

TESTING HIGH DENSITY PC BOARD ASSEMBLIES

Because the component density may be equal on both primary and secondary sides of the assembly, conventional electrical testing for process monitoring may not seem practical or possible. The small via pads typical on the high density fine pitch or uBGA PC board can be utilized for test probe access however, test specialist generally request enlargement of specific pads (see Figure 3) needed for probe contact.

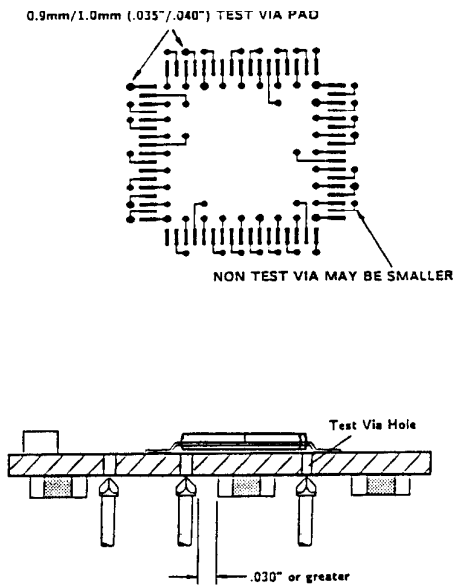


Figure 3. Small via pads designated for test probe access should be enlarged to 0.9mm (.035") minimum to provide a reliable contact.

Electrical models are developed in the test system's software for each device type. If test probe contact patterns are not accessible at each common junction of the circuit network then measuring or exercising the components (individually) during the test is not possible. Of particular concern on fine pitch or Micro BGA assemblies is the accessibility for probing at all of the circuit nets or common connections between devices with automated test systems. When the design does not meet this "net access" requirement, reliable and consistent electrical testing may be compromised and assembly process defects or damaged device detection cannot be identified until functional test.

DETERMINE MOST EFFICIENT ASSEMBLY PROCESS

One assembly process for all surface mount applications is not always practical and depending on the device mix, density and assembly complexity, two or more assembly methods may be employed.

SURFACE MOUNT ASSEMBLY COMPLEXITY

- o SMT on One Side Only
- o SMT on Two Sides
- o SMT and Fine Pitch/uBGA on One Side
- o Two Side SMT, QFP/uBGA on One Side
- o Two Side SMT, QFP/uBGA on Two Sides

The overall component density factor and higher percentage use of fine pitch devices on high performance electronic

products adds a unique level of difficulty to the assembly process (as well as test and inspection).

Recognizing that Fine Pitch/uBGA design is a more complex assembly than the average surface mount product, assembly process refinement may be considered to ensure manufacturing efficiency and yield.

As complexity of assembly processing increases the cost of assembly increases. For example, before locating fine pitch, ball grid array or die size Micro BGA devices on both primary and secondary sides of the board, the designer should understand the associated difficulty factor for both design layout and assembly processing. Other issues to be considered are the unique attachment process methods required for other device technologies. PC board assemblies are not always exclusively surface mount and often, a mix of leaded pin-in-hole (PIH) components are included in the design. In an automated in-line assembly operation, surface mount devices are generally (but not exclusively) attached with a reflow solder process.

The most efficient method of processing an assembly with both SMT and PIH device technologies may include reflow and wave solder. When both reflow and wave processes are employed, leaded PIH devices are installed during the final assembly operations. That is, termination of leaded devices is most often fulfilled following the reflow soldering of surface mount devices using a wave or other solder process.

SOLDER ATTACHMENT

Although other attachment materials are available for assembly of electronic products, solder alloy attachment of devices is most common method in use. Reflow soldering is a process that uses a tin/lead alloy supplied in a paste like form. The paste material converts to a liquid when exposed to temperatures exceeding 190°C. The reflow solder process uses a non contact heat transfer technology, typically infrared, forced convection (hot air or gas) or vapor phase. As noted, wave solder can be used to attach both leaded and selected surface mount devices but surface mount devices exposed to the molten solder must be attached to the boards surface with an epoxy before soldering.

After reviewing the device types selected, their location and the general complexity of the assembly, process engineers will develop a detailed manufacturing plan. The plan will identify the most cost effective methods for assembly and include the solder attachment processes to be employed. One of the following in-line solder process options may be considered:

SOLDER PROCESS OPTIONS

- o Reflow Solder
- o Double Reflow Solder

- o Reflow/Wave Solder
- o Double Reflow/Wave Solder
- o Double Reflow/Selective Wave
- o Reflow Solder w/ Ruppert Process

The reflow/wave and double reflow/wave solder process requires epoxy attachment of all surface mount devices on the secondary side of the board (devices exposed to the molten solder). The designer should use caution when considering wave solder for active device attachment because many surface mount component types (J lead, Fine Pitch and Ball Grid Array or uBGA devices for example) are not suitable for wave solder.

CONSIDERATIONS FOR SELECTIVE WAVE SOLDER

Selective wave solder process uses a pallet fixture that masks the previously reflow soldered devices from exposure to the molten material. The selective wave solder fixture is designed to secure the assembly and allow solder contact at specific locations.

When selective wave solder follows a double reflow solder process, specific clearances are defined between surface attached devices and the leads exposed to the wave solder. If devices previously attached during the reflow process can not be shielded from a secondary exposure to the wave solder sequence, epoxy must be dispensed under the exposed part before the reflow solder operation. In this way, the surface mount parts will stay in position although the attachment solder is returned to liquid when exposed to the wave.

To avoid the use of adhesive, physical clearance restrictions between the surface attached device and PIH device lead must be considered, allowing unrestricted exposure to the wave solder. Also, to avoid excessive fixture thickness, higher profile surface mount components, those with an overall height greater than 3.0mm (.125"), should be moved to the primary surface of the board.

REFLOW SOLDER OF PIH DEVICES

The Ruppert Process allows the manufacturing engineer a method for simultaneously reflow soldering surface mount and leaded PIH devices. In this process, a calculated volume of solder paste is deposited in a pattern around each lead hole and pad feature. As the solder converts to liquid, the alloy flows to the lead, filling the hole and furnishing a very consistent solder joint. When adapting this process, components must be selected that can physically withstand the temperature of reflow soldering.

MANUFACTURING PROCESS INSTRUCTIONS (MPI)

Because detail drawings are often large and awkward to handle on the production floor, process engineering will typically prepare unique instructions for each phase of the assembly operation. The preparation of a detailed

Manufacturing Process Instruction (MPI) document and the use of specific fixture technology, both production yield and cost objectives can be met. The MPI can be developed for production floor use as hard copy instructions or distributed electronically. Because copy machines are so common in business environments, timely implementation of changes and retrieving or replacing all obsolete (or down rev) hard copy from a large production operation can be difficult. Adding an expiration date or time to all documents on the production floor is recommended. Electronic distribution of documentation has proven to be an advantage over hard copy when rapid response to engineering change (EC) is critical.

PANELIZATION FOR MACHINE TRANSFER

PC Board shape and size will impact both fabrication cost and assembly efficiency. In order to automate the transfer of a board from one assembly station to another, provisions can be made to accommodate conveyer systems. Small or odd shaped boards for example, are more efficiently processed in a panel array. These individual assemblies can be retained in an efficient panel array format and after all the assembly process steps are concluded, excised by hand or machine (see Figure 4).

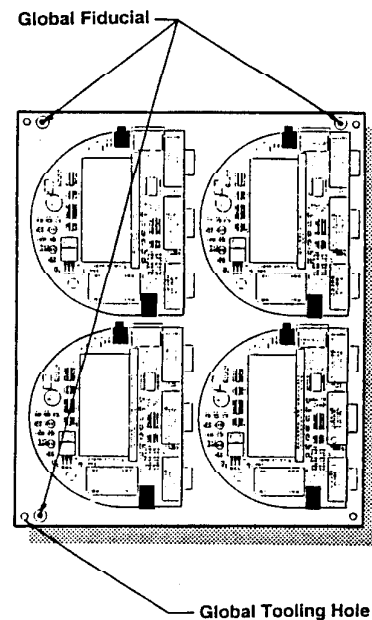


Figure 4. Small and/or irregular shaped PC Boards are furnished in a uniform panel format for efficient handling during assembly automation processes. The individual assembly units are separated following soldering and cleaning operations.

Panelization can apply to larger boards as well. Even though the board outline specified for the finished assembly is an

irregular shape, additional board material can be retained to furnish at least two uniform parallel sides.

PCB MATERIAL PLANNING

Panel size limits must also be considered. To control the cost of the bare board the designer must attempt to maximize material usage yield the highest possible quantity of finished boards from a standard panel blank. As an example, 18" x 24" panel blanks typical of that shown in Figure 5 are common for domestic multilayer PCB suppliers.

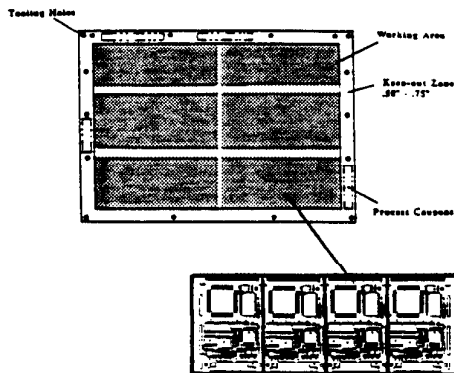


Figure 5. When developing the panel array, maximum utilization of the fabrication process panel will avoid or reduce excessive waste of PC board material.

Other panel sizes are available but the 18" x 24" panel size is most common due to the laminating press design. The actual usable area for the 18" x 24" size noted may be only 16" x 22" depending on boarder areas reserved for alignment pins and test coupons. Assembly machines have panel size restrictions as well. Some models of Panasonic and Fuji assembly systems for example, can only accommodate a panel size of 14" x 18" while other systems may accept a panel measuring 18" x 20" or more.

ASSEMBLY EQUIPMENT (PCB SIZE) LIMITATIONS

When the SMT product requires large finished board sizes, the designer will need to know the assembly equipment limitations *before starting CAD design*. In addition to panel size limits and specific tooling hole requirements there are other physical restrictions or features that must be considered during the design phase of a program. The conveyer transfer mechanism on stencil machines, dispensing systems and placement equipment requires a minimum clearance from board edge to component body or land pattern of 3.1mm (.125"). Tooling hole size and location will also vary somewhat between assembly systems. The Fuji and Panasonic systems, for example, specify two non-plated tooling holes on a line parallel to the long edge of the board.

The holes are positioned 5.0mm (.200") from the board edge and an equal dimension from each end.

The more sophisticated assembly machines use automated vision systems for precise alignment adjustment for both solder paste application and device placement. To accommodate the vision features, the designer must provide fiducial targets on the board surface. The fiducial target is etched into the board to minimize dimensional tolerance accumulation to the land pattern geometry provided for device attachment. Three global fiducial targets are required for each board side having surface mount devices. Two addition fiducial targets for each fine pitch device is requested as well. The standard (minimum) size of the target is 1.0mm (.040") diameter with a clearance of 0.25-0.50mm, void of solder mask and other physical features (see Figure 6).

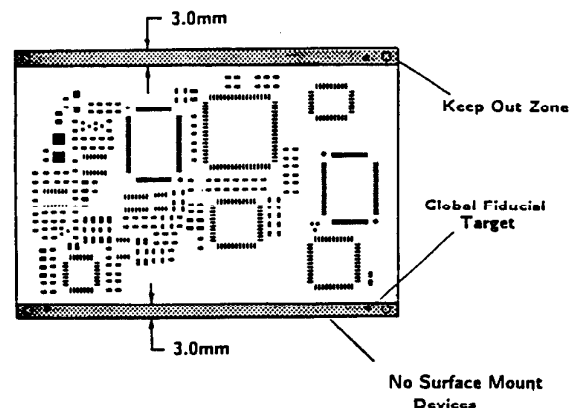


Figure 6. To accommodate the vision alignment systems on surface mount assembly equipment, each board or panel must include three global fiducial targets (and two fiducial patterns for each fine pitch device).

The standard fiducial is a solid filled etched copper circle .040" (1.0mm) in diameter. A clear zone must be provided around the fiducial diameter and devoid of any other circuit features as well as solder mask material.

DOCUMENTATION FOR FIXTURE DEVELOPMENT

Development of PCB assembly fixtures requires detailed instructions as well as CAD data. Before releasing the product to assembly, documentation must be complete and accurate. The Gerber or IPC-D-350 data generated to fabricate the PC Board can be used to assist in assembly machine programming, development of solder stencils and other assembly and test fixtures. Even though each assembly system may use incompatible software, equipment companies or system specialists have developed the conversion or translation software features to adapt the standard CAD data into a compatible format.