

Jitter Characteristics and Measurements



Introduction

Transferring digital signals from one location to another involves converting the signals into an analog physical representation at the sending end and then interpreting that representation to extract the data at the receiving end. This is necessary because any signals that are physically represented inherently have analog properties. These properties include the levels and timing of the data intervals and the transitions between them, the spectral distribution that results, and any signal distortions that occur in the transmission system. This is true whether the signals are modulated onto an RF carrier or transmitted directly as data using an appropriate form of encoding.

Analog effects that can alter digital signals are attenuation, spectral roll-offs and anomalies, overshoots, undershoots, time dispersion, and jitter. The first several are frequency- and amplitude-related effects while jitter is the sole timing-related disturbance.

1 Scope

This guideline examines the types of jitter in directly transmitted data signals, the methods for measuring each one, and some of the impacts they can have on system operation. Additionally, some of the system design approaches that can minimize or mitigate the impact of jitter are presented.

2 Jitter definition

In this guideline, the 270 Mbits/s (Mb/s) serial digital interface (SDI) signals of SMPTE 259M will be used as an example, but the same concepts apply to serially transmitting everything from 3.1 Mb/s AES3 audio data streams through 1.5 Gb/s HDTV versions of the SDI. Only the numerical values used for equipment specifications and measurements change when covering this large range of digital signals.

To send digital data streams from one place to another over a single wire or fiber, data is encoded using one of several self-clocking methods. These include such schemes as NRZ, NRZI, bi-phase mark, and others which typically trade-off the resulting data signal bandwidth and spectral shaping for ease of clock extraction, error detection ability, or other performance features. The important thing about all of these designs is that they allow the clock to be extracted from the data stream so it can be used to recover the data.

Clocking information is usually extracted using phase lock loop circuits. The transition locations in a data stream are instantaneously compared with transitions of a synthesized clocking signal coming from a local oscillator (typically an RC- or LC-type voltage controlled oscillator) at the receiver. The local clock's frequency is then adjusted up or down until the extracted clock's edges agree with the incoming data edges. This process is straightforward as long as the data transitions occur at the expected intervals; that is, integer multiples of the serial clock period. In real systems, however, the data transitions will deviate somewhat from their ideal position; that is, the pulse positions vary with respect to a high stability frequency-locked clock. This unwanted pulse position variation is jitter.

Jitter is defined as the variation of a digital signal's significant instants (such as transition points) from their ideal positions in time. Jitter can cause the recovered clock and the data to become momentarily misaligned in time. Data may be misinterpreted (latched at the wrong time) when this misalignment becomes great enough. Jitter is measured in terms of the unit interval (UI), which represents the period of one clock cycle and, for NRZ or NRZI encoded data, corresponds to the nominal minimum time between transitions of the serial data. This can be seen in figure 1a, where the data of an NRZI signal and the related clock ticks are shown. Figure 1b shows the effect of jitter on the midpoint crossings of the data transitions, as would be seen on an eye-pattern presentation (repetitive display of transition points overlaid upon one another). Increasing jitter closes the eye in the time dimension and makes decisions between data states correspondingly more difficult, just as signal voltage noise does in the amplitude dimension.

Jitter, then, can be thought of as the phase variation (or modulation) of the serial data stream. This phase modulation has a spectrum that corresponds to the frequency with which the data's clock is modulated. Thus, it is possible to plot an amplitude versus frequency characteristic of the jitter. For example, in figure 2, a single spike at 6144 Hz indicates the presence of sinusoidal phase variation (jitter) at a rate of 6144 Hz. The amplitude of the spike would indicate how much of the data eye was closed.

3 Classes of jitter

Absolute jitter is the aggregate of all jitter frequency components found in a signal, from very low to very high frequency. Measuring exact absolute jitter is practically impossible because it is difficult to generate an absolute reference defining where data edges should be. The practical study of jitter divides it into three classes, based on the frequency content of the jitter modulation.

The very lowest frequency variations in the positions of a signal's transitions are termed wander. Wander typically has no effect on the capability of the clock extraction and decoding electronics to accurately recover the digital data stream because this low-frequency variation can be followed by the PLL (unless the wander causes the data rate to go outside the range of the controlled reference oscillator).

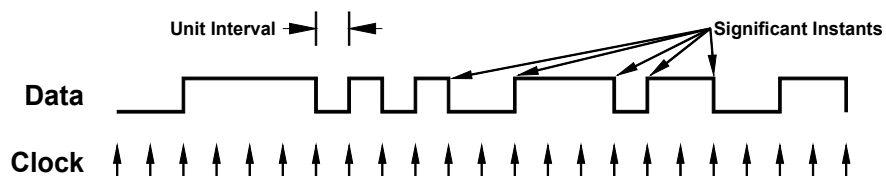
Wander may, however, cause problems in later downstream processing. Wander is generally defined as jitter with frequency components below a particular frequency. In SDI applications, this assigned cutoff is 10 Hz. Measuring wander and absolute jitter implies that the clocking reference used to identify edge jitter be extremely stable with no jitter component of its own. Typical PLL-extracted clocks are unsuitable for this measurement. The source of such an accurate reference signal might be a high-Q crystal oscillator; however, access to this type of signal is not common in SDI applications. This limitation typically causes wander to be excluded in jitter measurements.

Jitter that occurs above the highest frequency defined as wander is termed timing jitter. Jitter that is measured relative to a recovered clock with a loop bandwidth defined by f_3 (figure 3) is called alignment jitter. The difference between timing jitter and alignment jitter is the low-frequency jitter.

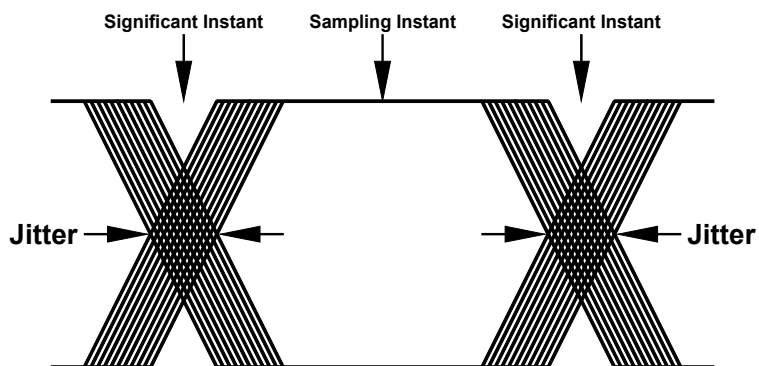
The timing jitter measurement is used to provide an idea of how the overall system is performing. It can be measured by setting the loop filter bandwidth of the clock recovery system to f_1 . The result will include all frequencies of jitter above the loop filter cutoff to the upper limit of the measurement. This broadband measurement will not specifically identify jitter that could cause data recovery errors.

Alignment jitter can provide information on jitter that directly affects the receiver's ability to properly recover data. This type of error occurs because the PLL is not able to track the timing changes of the incoming signal. If the timing errors become large enough, the decoder will "slip" a bit, which will cause an error in the decoded data. This produces a word framing error, which will not be corrected until the next timing reference signal.

Low-frequency jitter generally does not cause problems in the serial link. Large amounts of low-frequency jitter can be tolerated by the serial link, as the PLL follows these timing changes and maintains proper data recovery. However, one must be aware of this band of jitter, as it will be present in the recovered parallel clock. This parameter is important to monitor if the recovered clock is to be used as a reference signal in the parallel domain.



a) Relationship of Data & Clock for SDI Signals
Showing Unit Interval & Significant Instants



b) Eye Pattern Showing Jitter at Significant Instants

Figure 1 – Elements of serial data signals and relationship to jitter

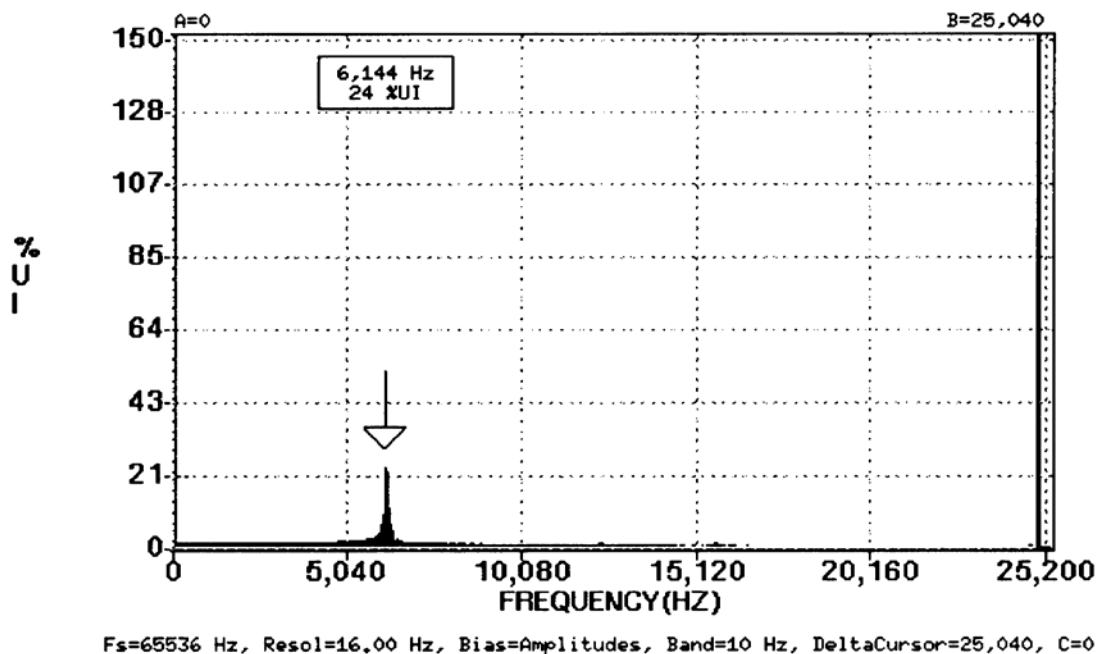


Figure 2 – Jitter frequencies

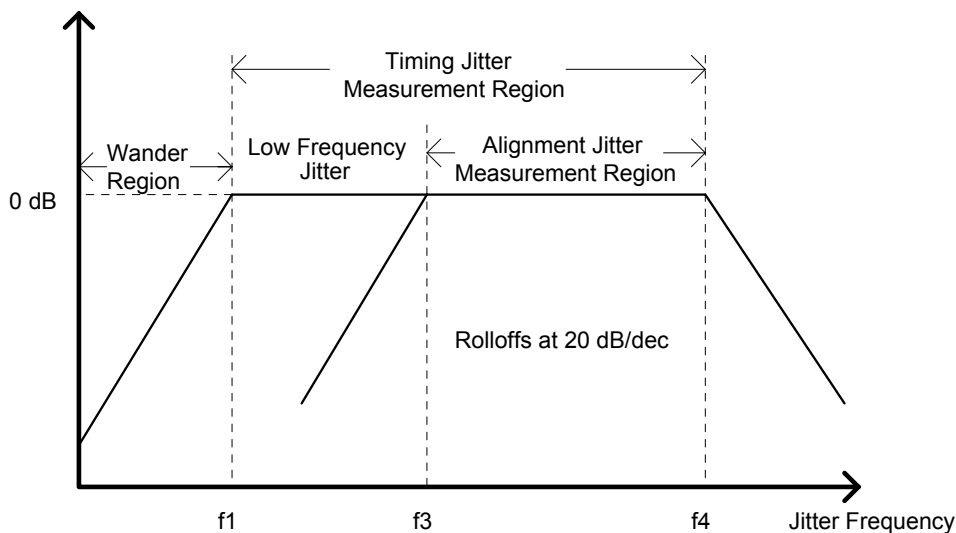


Figure 3 – Jitter measurement regions

The low-frequency jitter can be found by subtracting the alignment jitter from the timing jitter. This will yield accurate results for most types of jitter, such as sinusoidal or random sources of jitter. If the jitter source is a complex waveform, such as a square wave, the frequency and duty cycle will have an effect on this calculation.

In the case of SMPTE 259M serial digital video applications, the frequency roll-off definition for alignment jitter measurements (f_3) is 1 kHz. Because there are many popular SDI receivers already in use throughout the industry, this value had to be chosen to be useful for all systems. When choosing this number, a frequency high enough to ignore jitter from typical gen-lock circuits (200 Hz or greater) and low enough to include the clock recovery bandwidths for all popular receiver integrated circuits (10 kHz or less) had to be found.

4 Jitter measurements

Several different instruments and connection arrangements can be used to measure jitter of various types. The more complex techniques will produce more informative results, but the simpler methods can be meaningful as a starting point for understanding the jitter types occurring in a particular system.

The simplest method for observing and measuring jitter is the use of an oscilloscope with an external reference for triggering, as shown in figure 4. The SDI source and the external reference must be locked to a common clock, as any frequency difference (which is not jitter) may interfere with the measurement. The spread of the crossing points of an eye display will reveal the jitter amplitude. If a highly stable external reference, such as a clock derived from black burst, is used, absolute jitter, including wander, will be displayed.

When an external triggering reference is not available, a reference clock must be extracted from the data itself. In this way, greater detail regarding the characteristics of the jitter can be obtained. This can be done by using a clock extractor. A clock extractor is a device that recovers a reference clock from the incoming data stream. The block diagram of a representative clock extractor is shown in figure 5. Clock extractors phase lock to the data stream to synthesize a reference clock and this process inherently has a frequency response to it. A clock extractor that has a phase lock loop natural frequency of 1 kHz will only measure jitter frequencies above 1 kHz because the synthesized reference clock extracted from the data will track the frequency variations at rates below 1 kHz. For this reason, clock extractors typically support multiple-loop filter roll-off frequencies.