

SMPTE RECOMMENDED PRACTICE

Specification of Jitter in Bit-Serial Digital Systems



Page 1 of 18 pages

Table of Contents	Page
Foreword	2
Intellectual Property	2
Introduction.....	2
1 Scope	3
2 Conformance Notation	3
3 Normative References	3
4 Definitions	4
5 Jitter Specifications	5
5.1 Input Jitter Tolerance	5
5.2 Jitter Transfer	8
5.3 Intrinsic Jitter and Output Jitter	9
Annex A Terminology Changes (Informative)	12
Annex B Derivation of Probabilistic Peak-to-Peak Jitter (Informative).....	13
Annex C Bibliography (Informative)	18

Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally-recognized standards developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE's Engineering Documents, including Standards, Recommended Practices, and Engineering Guidelines, are prepared by SMPTE's Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

SMPTE Engineering Documents are drafted in accordance with the rules given in its Standards Operations Manual.

SMPTE RP 184 was prepared by Technology Committee 32NF.

Intellectual Property

At the time of publication no notice had been received by SMPTE claiming patent rights essential to the implementation of this Engineering Document. However, attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. SMPTE shall not be held responsible for identifying any or all such patent rights.

Introduction

This section is entirely informative and does not form an integral part of this Recommended Practice.

This Recommended Practice (RP) defines the parameters for measuring jitter in serial digital video systems. The companion SMPTE RP 192 defines the methods and architectures of the measuring equipment. The intent of these two RPs is to allow equipment manufactures to make consistent measurements that reflect system performance, and to educate users on how to evaluate systems.

1 Scope

This Recommended Practice describes techniques for specifying jitter in self-clocking, bit-serial digital systems. It is applicable to sources, receivers, and regenerators. It is specifically intended for, but not limited to, 270 Mb/s to 12 Gb/s serial systems as defined by: SMPTE ST 259, SMPTE ST 292-1, SMPTE ST 424, SMPTE ST 435-3, SMPTE ST 2036-4, SMPTE ST 2081-1, and SMPTE ST 2082-1. Methods for measuring these specifications are found in SMPTE RP 192.

2 Conformance Notation

Normative text is text that describes elements of the design that are indispensable or contains the conformance language keywords: "shall", "should", or "may". Informative text is text that is potentially helpful to the user, but not indispensable, and can be removed, changed, or added editorially without affecting interoperability. Informative text does not contain any conformance keywords.

All text in this document is, by default, normative, except: the Introduction, any section explicitly labeled as "Informative" or individual paragraphs that start with "Note:"

The keywords "shall" and "shall not" indicate requirements strictly to be followed in order to conform to the document and from which no deviation is permitted.

The keywords, "should" and "should not" indicate that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain possibility or course of action is deprecated but not prohibited.

The keywords "may" and "need not" indicate courses of action permissible within the limits of the document.

The keyword "reserved" indicates a provision that is not defined at this time, shall not be used, and may be defined in the future. The keyword "forbidden" indicates "reserved" and in addition indicates that the provision will never be defined in the future.

A conformant implementation according to this document is one that includes all mandatory provisions ("shall") and, if implemented, all recommended provisions ("should") as described. A conformant implementation need not implement optional provisions ("may") and need not implement them as described.

Unless otherwise specified, the order of precedence of the types of normative information in this document shall be as follows: Normative prose shall be the authoritative definition; Tables shall be next; followed by formal languages; then figures; and then any other language forms.

3 Normative References

The following standards contain provisions which, through reference in this text, constitute provisions of this recommended practice. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this recommended practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

No references are cited in this document.

4 Definitions

4.1 Alignment jitter

The variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

4.2 Independent Samples

For band-limited systems, samples are only independent if they are not over-sampled. By the Nyquist criteria this means that for a given bandwidth in Hz, the maximum number of independent samples per second is approximately twice the bandwidth. Any higher rate of samples will be just giving more information about the same signal components

4.3 Input jitter tolerance

Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

4.4 Intrinsic jitter

Jitter at an equipment output in the absence of input jitter.

4.5 Jitter

The variation of a digital signal's transitions from their ideal positions in time.

4.6 Jitter transfer

Jitter on the output of equipment resulting from applied input jitter.

4.7 Jitter transfer function

Ratio of the output jitter to the applied input jitter as a function of frequency.

4.8 Output jitter

Jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

4.9 Probabilistic Peak-to-Peak Jitter (p-p-p, Stated as Jitter at 1 in 10^x)

This is an estimate of the most likely p-p jitter in unit intervals when measured over 10^x independent jitter samples. See Annex B for derivation.

4.10 Timing jitter

The variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

4.11 Unit interval (UI)

Abbreviated UI, it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

5 Jitter Specifications

Equipment jitter specifications fall into three categories: input jitter tolerance, jitter transfer, and intrinsic jitter. A fourth specification, output jitter, is a system specification and may be used to specify jitter limits at equipment interfaces.

At most device outputs in a SDI system, the observed jitter will be output jitter, consisting of the device's intrinsic jitter and any jitter transfer term from the signal driving the device. Output jitter will be at least as large as intrinsic jitter, and may be much greater in cases where there is a significant jitter transfer term. At the time of this publication, the serial interface standards SMPTE ST 259, SMPTE ST 292-1, SMPTE ST 297, SMPTE ST 424, SMPTE ST 435, SMPTE ST 2036-4, SMPTE ST 2081-1 and SMPTE ST 2082-1 only specify intrinsic jitter.

Note: System designers are encouraged to define the desired system jitter margin and the allowed output jitter at each point in the system, given the jitter transfer and input jitter tolerance of the devices being used, so that the desired system error performance is reliably achieved. Cascading serial devices can lead to jitter accumulation. The characteristic of the jitter accumulation depends on the architecture of the serial devices:

- Many devices implement a reclocker with a very low frequency loop bandwidth, or use an internal or external frequency reference to effectively prevent all input jitter from passing through to the output.
- Other reclocking devices have a moderate loop bandwidth for the reclocking function, they attenuate jitter well above this bandwidth and pass through any jitter well below this bandwidth. At jitter frequencies near the loop bandwidth, reclockers may peak up and amplify input jitter. In addition, reclockers have a jitter contribution of their own that may add to the low frequency jitter they pass through from the input, and which is typically the main source of high-frequency jitter on the reclocker output.
- Devices without reclocking pass all input jitter and can add jitter at any frequency.
- Cascading multiple devices of the same type can lead to exaggerated effects; e.g., if several reclockers have peaking at the same frequency. Some devices are not prone to this behavior.

5.1 Input Jitter Tolerance

Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. Input jitter tolerance is applicable to most serial inputs.

Input jitter tolerance requirements are specified with a jitter template that covers a specified sinusoidal amplitude/frequency region (see Figure 1). This template represents the minimum amount of jitter that the equipment must accept without causing the specified degradation of error performance. Equipment meeting a jitter tolerance requirement must have an actual jitter tolerance greater than the requirement (see Figure 2).

Input jitter tolerance requirements are specified with the parameters given in Table 1.

Frequency band f_1 to f_2 forms the low-frequency jitter tolerance bandpass. At least A_1 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

Frequency band f_3 to f_4 forms the high-frequency jitter tolerance bandpass. At least A_2 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

A_1 and A_2 shall be specified in UI.

The slope of the jitter tolerance requirement between f_2 and f_3 shall be 20 dB/decade. Frequencies f_2 and f_3 are related as follows: $F_2 = f_3/(A_1/A_2)$.

The criterion for reaching the onset of errors shall be specified. Either a BER limit or a maximum number of errored seconds over a specified measurement interval should be used.

The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

Numerical input jitter tolerance values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with Table 1.

Table 1 – Input jitter tolerance

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f1	(Hz)	(Low-frequency specification limit)
f2	(Hz)	(Upper band edge for A1, low-frequency jitter tolerance)
f3	(Hz)	(Lower band edge for A2, high-frequency jitter tolerance)
f4	(Hz)	(High-frequency specification limit)
A1	(UI)	(Low-frequency jitter tolerance, f1 to f2)
A2	(UI)	(High-frequency jitter tolerance, f3 to f4)
Error criterion		(Criterion for onset of errors)
Test signal		(Test signal used for measurement)

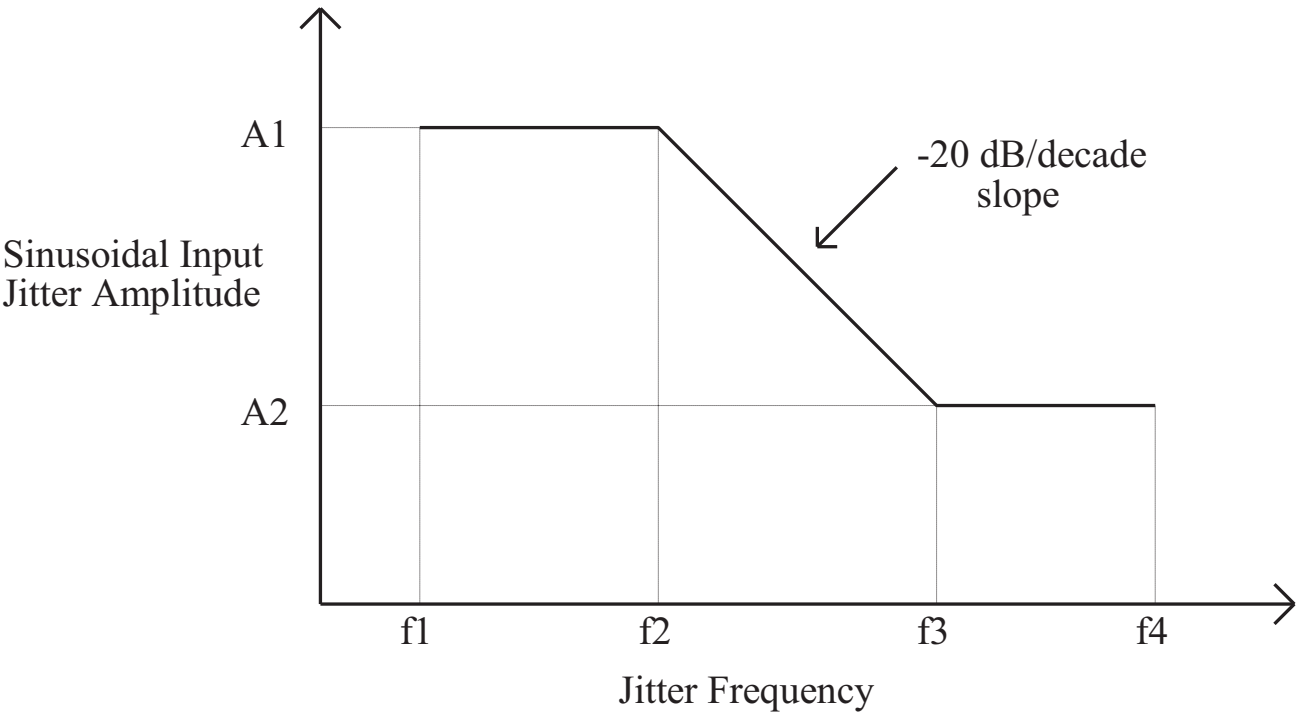


Figure 1 – Input jitter tolerance template