

SMPTE RECOMMENDED PRACTICE

Jitter Measurement Procedures in Bit-Serial Digital Interfaces



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1 Scope

1.1 Scope

This practice describes methods for measuring jitter performance in bit-serial digital interfaces. The techniques are specifically suited for jitter specifications that follow the form described in SMPTE RP 184.

1.2 Introduction

Jitter is one of the most important parameters in the performance of serial digital transmission systems. It can cause errors in the transmission and recovery of digital data, and may degrade analog signal performance if the jitter is transferred through the digital-to-analog conversion process. Characterizing and measuring jitter are important for reliable and predictable serial digital system operation.

2 Normative reference

The following standard contains provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the edition referenced was valid. All standards are subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below.

SMPTE RP 184-1996, Specification of Jitter in Bit-Serial Digital Systems

3 Definitions

3.1 alignment jitter: Variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 clock extractor: A device which is able to extract the serial data clock from a serial data stream, and outputs a clock-related trigger. It may also provide the serial digital data reclocked with the extracted clock.

3.3 DSO: Acronym for digital storage oscilloscope.

3.4 DUT: Acronym for device under test.

3.5 error rate tester: A device that quantifies the error rate of a serial digital signal. Two examples are the classic bit error rate (BER) tester and the field rate CRC method (EDH) described in SMPTE RP 165.

3.6 input jitter tolerance: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.7 intrinsic jitter: Jitter at an equipment output in the absence of input jitter.

3.8 jitter: Variation of a digital signal's transitions from their ideal positions in time.

3.9 jitter generator: A device which produces a serial digital signal containing sinusoidal jitter of adjustable amplitude and frequency.

3.10 jitter receiver: Demodulates and allows measurement of the jitter present on a serial signal. It commonly provides an output proportional to the demodulated jitter.

3.11 jitter transfer: Jitter on the output of equipment resulting from applied input jitter.

3.12 jitter transfer function: Ratio of the output jitter to the applied input jitter as a function of frequency.

3.13 output jitter: Jitter at the output of equipment that is embedded in a system network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.14 phase demodulator: A device that provides as its output a signal proportional to the phase difference of two input signals.

3.15 SDI: Acronym for serial digital interface, typically referring to an ANSI/SMPTE 259M system.

3.16 timing jitter: Variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.17 unit interval (UI): Abbreviated "UI", it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specification

Four methods are described: The first uses an available reference clock to trigger an oscilloscope; the second uses a clock extractor with defined characteristics to trigger the oscilloscope; the third and fourth are based on a phase demodulator method jitter receiver.

4.1 Oscilloscope measurement by means of triggering on a reference signal

If a reference signal is available, a basic jitter measurement can be done (see figure 1). The oscilloscope is directly triggered by the reference signal. This reference signal could also be a serial digital signal with high stability. The digital data signal is connected to the suitably terminated vertical channel of the oscilloscope and an eye measurement is done. The jitter is typically measured at the eye crossing.

– Presentation of measurement results: The test signal, the jitter amplitude, the parameters of the oscilloscope (bandwidth, etc.), and the measurement time should be indicated.

– Background information: This measurement procedure provides a coarse survey of jitter in an SDI signal. The measurement result depends on the stability of the reference signal (its jitter sets the measurement floor), the type of oscilloscope, and the measurement time (e.g., when a DSO is used in persistence mode). All of these parameters influence the measurement result and contribute to variability in the result as conditions vary. This method does not allow bandwidth restriction as generally required in jitter specification. This method is not recommended if other jitter measurement methods are available.

4.2 Jitter measurement by means of a clock extractor

The jitter in a signal output can be measured by using a device to extract a clock and then trigger an oscilloscope or other indicating device (see figure 2).

4.2.1 Clock extractor block diagram

The clock extractor typically consists of a wideband clock recovery circuit followed by a second, narrow band PLL (see figure 3). This second PLL can be set to two different loop bandwidths, so that two different jitter transfer functions are available (see figure 4). Clock output 2 is used to trigger the indicating device. The clock extractor shall have the following characteristics:

- 1) It shall be capable of being put in series with the signal output and provide enough signal level for the indicating device. It shall not modify the output signal characteristics in ways that obscure or modify the jitter on the signal.
 - 2) To measure timing jitter (A1), the clock extractor shall have a clock recovery bandwidth of f_1 . To measure alignment jitter (A2), the clock extractor shall have a clock recovery bandwidth of f_3 (see figure 4). The number of integrations within the clock extractor PLL shall be at least two (TYPE II PLL) to provide at least a 40 dB/decade attenuation to wander or low-frequency jitter in the following jitter indication devices of 4.2.2.
- NOTE – A three integrator PLL (TYPE III) is preferred providing 60 dB/decade wander attenuation. However, since these are more difficult to design, a Type II is acceptable.
- 3) The jitter transfer function of the clock extractor shall roll-off at 20 dB/decade or greater and have a minimum phase response unless otherwise specified. Ripple within the pass band shall be less than ± 1 dB (see figure 4).
 - 4) The extracted clock frequency shall be the serial clock frequency divided by n , where n is defined in 4.3.2 of SMPTE RP 184.
 - 5) The clock extractor may have an optional clock output 1, which has a clock recovery bandwidth f_{cr} greater than or equal to f_3 . It is preferable that f_{cr} equal 14.

4.2.2 Indicating device specifications

The indicating device used to observe the jitter shall have the following characteristics:

- 1) The horizontal and/or trigger bandwidth of the indicating device shall not attenuate the observed jitter. The trigger bandwidth shall be at least f_3 .
- 2) The indicating device shall not create intersymbol interference at the zero-crossing point. This requires a vertical system step response that transitions and settles in less than 1 UI.
- 3) The indicating device shall acquire sufficient samples so that peak-to-peak jitter can be determined. This requires sampling until the shape of the jitter distribution is known. If the jitter specification includes a measurement time, this shall be the minimum acquisition time. The maximum acquisition time will depend on the device sample rate and the type of jitter distribution. For example, a sinusoidal distribution will typically be determined with fewer samples than will a gaussian-like distribution.

NOTE – The minimum required measurement time depends on how quickly the measurement device collects samples. For digital storage oscilloscopes (DSOs), this is determined by the acquisition rate and the number of samples per acquisition. While the latter term is related to the advertised DSO sample rate, the former is not. DSOs with identical sample rates may take very different amounts of time to build a sufficient sample record to make a measurement.

The minimum measurement for a given oscilloscope may be determined as follows: First, have the scope acquire for a very long time to establish the jitter level. Then, successively shorter measurements are taken until the results start showing unacceptable error or variation. This establishes the minimum measurement time for the scope. Experienced users often have an intuitive feeling for this value based on how the sample distribution is filling in.

4) If the indicating device is an oscilloscope, the jitter measurement is usually made at the eye crossing. A digital storage oscilloscope with infinite persistence is recommended.

4.2.3 Measurement of timing jitter

The clock extractor is set to bandwidth f_1 . The clock output 2 is connected to the trigger channel of the oscilloscope. The signal connected to the oscilloscope vertical channel depends on the jitter amplitude being measured. For jitter amplitudes less than 1 UI, the loop-through signal is used (see figure 2). For jitter amplitudes greater than 1 UI, two different connections are possible:

1) (Preferred) If the clock extractor has a clock 1 output (figure 3), this signal is applied to the oscilloscope vertical channel (see figure 5). This connection will ensure jitter between frequencies f_1 and f_{cr} , where f_{cr} is the bandwidth of the wideband clock recovery circuit.

2) If the clock extractor has simultaneous outputs at bandwidths f_1 and f_3 , one output is connected to the vertical channel and the second to the trigger. This connection measures jitter between frequencies f_1 and f_3 .

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

4.2.4 Measurement of alignment jitter

The clock extractor is set to bandwidth f_3 . The clock output 2 is connected to the trigger channel of the oscilloscope. The loop-through signal is connected to the oscilloscope vertical channel (see figure 2).

– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.