

SMPTE RECOMMENDED PRACTICE

Solid State Media (SSM) Card Specification



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Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally-recognized standards developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE’s Engineering Documents, including Standards, Recommended Practices and Engineering Guidelines, are prepared by SMPTE’s Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

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SMPTE Recommended Practice 2006 was prepared by Technology Committee V16.

1 Scope

This document defines the specification of the Solid State Media (SSM) Card. The physical specification provides the physical characteristics of the Card and the connector. The electrical interface between a host and the Card is a high performance bus and this document specifies the signal description, the electrical characteristics, and the bus operations. The register specification defines the registers for configuration and also defines the specific registers related to interrupt signals or commands. The command specification defines the commands for the bus master data transfer and the sensing log information written in the SSM Card in addition to the ATA commands. To guarantee the performance of the SSM Card, requirements for writing and reading speed are specified. The file system for the SSM Card is the FAT system.

2 Normative references

The following standards contain provisions, which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI INCTIS 361-2002, AT Attachment with Packet Interface -6 (ATA/ATAPI-6)

PCI Local Bus Specification Revision 3.0 (Note: The Bylaws of PCI-SIG (section 15) limit the RAND licensing terms to members.)

FAT: ISO/IEC 9293, Second Edition, 1994-1 I-I 5, Information Technology — Volume and File Structure of Disk Cartridges for Information Interchange

3 Symbols and abbreviations

For symbol definition and abbreviations, the reader is encouraged to study the PCI and ATA specifications. This document uses same terms defined in the mentioned standards and in other referenced documents.

ATA	AT Attachment
ATAPI	AT Attachment with Packet Interface
FAT	File Allocation Table
PCI	Peripheral Component Interconnect
PCI SIG	PCI Special Interest Group

The following symbols and abbreviations are defined in the Physical specification.

N	Newton
WPS	Write Protect Switch

The following symbols and abbreviations are defined in the Electrical specification.

LV	Low Voltage
Vcc	Power
Vpp	Programming and peripheral voltages
GND	Ground
Agent	All devices which relates to a data transfer on the bus
Master	Device which drives the address bus and sends a command
Slave	Device which receives a command and responses to it
Assert	Set a signal active
Negate	Set a signal inactive
CCD	(SSM) Card Card Detect
CVS	(SSM) Card Voltage Sense
CCLK	(SSM) Card Clock which provides timing for all transactions
CAD	(SSM) Card Address and Data multiplexed bus - During the address phase, CAD contain a byte address. During the data phase CAD contain data.
CCBE	(SSM) Card Command and Bus Enables multiplexed bus — During the address phase CCBE are defined as bus Command. During the data phase, CCBE are used as Byte Enables.
CCLKRUN#	(SSM) Card Clock Request/Status
CDEVSEL#	(SSM) Card Device Select
CFRAME#	(SSM) Card Cycle Frame - While CFRAME# is asserted, data transfers continue.
CGINT	(SSM) Card Grant
CINT#	(SSM) Card Interrupt request
CIRDY#	(SSM) Card Initiator Ready
CPAR#	(SSM) Card Even Parity
CPERR#	(SSM) Card Parity Error
CREQ#	(SSM) Card Request
CRST#	(SSM) Card Reset
CSERR#	(SSM) Card System Error
CSTOP#	(SSM) Card Stop transaction
CTRDY#	(SSM) Card Target ready
Transaction	Bus cycle which is initiated by an address phase and is followed by data phases.

NOTE – The acronym “C” stands for (SSM) Card.

The following symbols and abbreviations are defined in the Register specification.

ABRT	Abort – Indicates the requested command has been aborted
BIST	Built-in Self Test
BSY	Busy – Indicates if a device is busy
DEV	Device select
DRDY	Device Ready
DRQ	Data Request – Indicates if data transfer is ready between a device and a host
EOT	End of Table
ERR	Error – Indicates an error occurred during execution of the previous command
IDNF	ID not found
INTA#	Interrupt A – used to request an interrupt
IRQ	Interrupt request bit which represents an INTRQ signal
IRQE	Interrupt request enable bit for IRQ
INTRQ	Interrupt request signal
nIEN	Enable bit for INTRQ signal
LBA	Logical Block Addressing – Addressing by the linear mapping of sectors
PIO	Programmed Input/Output
RO	Read only
Res	Reserved
R/W	Read/Write
WO	Write only
scatter/gather	Gathering scattered data from memory for transmission
SRST	Software Reset
UNC	Uncorrectable

The following symbols and abbreviations are defined in the Command specification.

CID	Card ID
CSD	Card Specific Data
DMA	Direct Memory Access

4 Introduction

Figure 4.1 shows the overall structure of the SSM Card specification and the relationship between the other reference documents and this document.

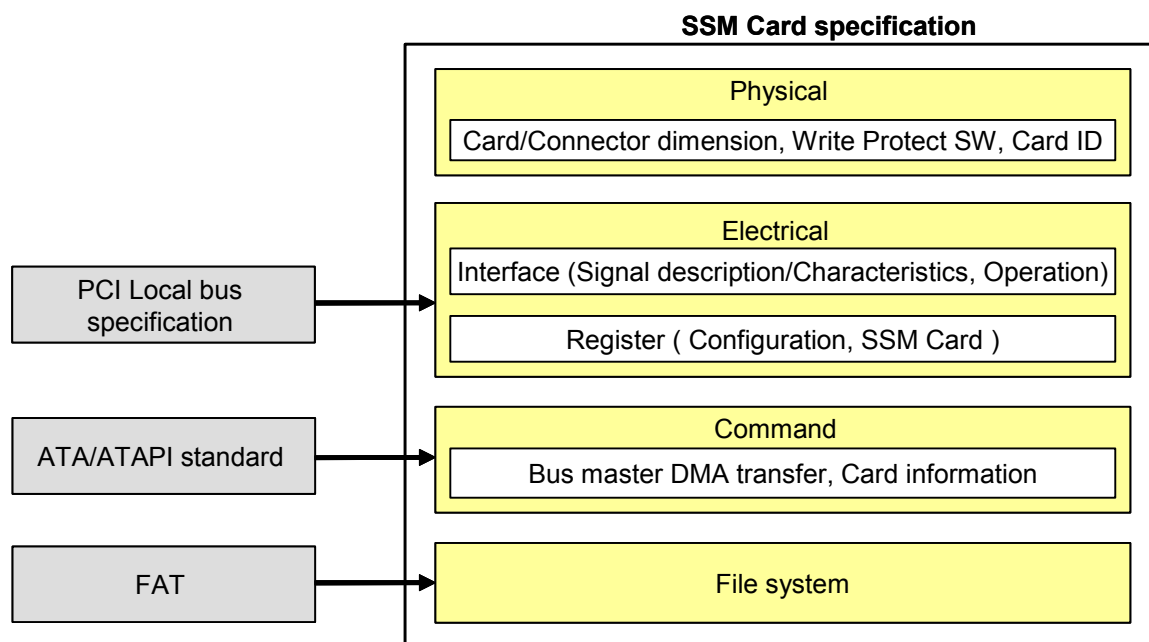


Figure 4.1 – Structure of SSM Card specification and relation between Reference documents

The physical specification defines the Card package dimensions, the Card connector, the write protect switch for protection of files stored on the SSM Card and the Card ID to identify the SSM Card.

The electrical interface of the SSM Card is a high performance 32 bit bus with multiplexed address and data lines. This document specifies the signal descriptions, the electrical characteristics and the bus operations of this SSM Card.

The register specification defines the Configuration space registers to identify or control the SSM Card and also defines the specific registers related to interruption or commands.

The command specifications define the commands required for the SSM Card. Write protection and power management are performed using ATA commands as unique functions for the SSM Card. Data transmission between a SSM Card and a host is performed using the Bus Master DMA transfer commands. After a read or write command is issued from the host, the SSM Card takes initiative of bus control and performs data transfers as the bus master. Furthermore, the commands for sensing log information written in the SSM Card are specified.

To guarantee the performance of the SSM Card, the writing and reading speeds required for the SSM Card are specified.

The SSM Card uses the FAT file system.

5 Physical specification

5.1 Card dimensions, socket configuration and pin numbering

Figure 5.1 specifies Card package dimensions. Figure 5.2 defines configuration of Card socket contacts and a relative pin contact locations, Figure 5.3 defines the pin connector layout and Figure 5.4 defines the pin connector dimensions.

5.2 Write Protect Switch and Card ID

The SSM Card shall be equipped with a Write Protect Switch (WPS) and Card Identification (Card ID).

The Write Protect Switch shall be located at the approximate position as shown in Figure 5.1. The status of the Write Protect Switch should be sensed by a host with the IDENTIFY DEVICE command (See 8.2) so that the host can perform the write protection functionality depending on the status of the Write Protect Switch.

The Card ID shall be located at the approximate position as shown in Figure 5.1.

5.3 Card Connector

The socket contacts on the SSM Card shall be located as specified in Figure 5.2.

The Card connector socket layout shall match the host pin-connector layout as shown in Figure 5.3.

The Card connector shall contain a top side planer, electrically conductive, ground plate with eight raised dimples 0.5 mm height as shown in Figure 5.4.

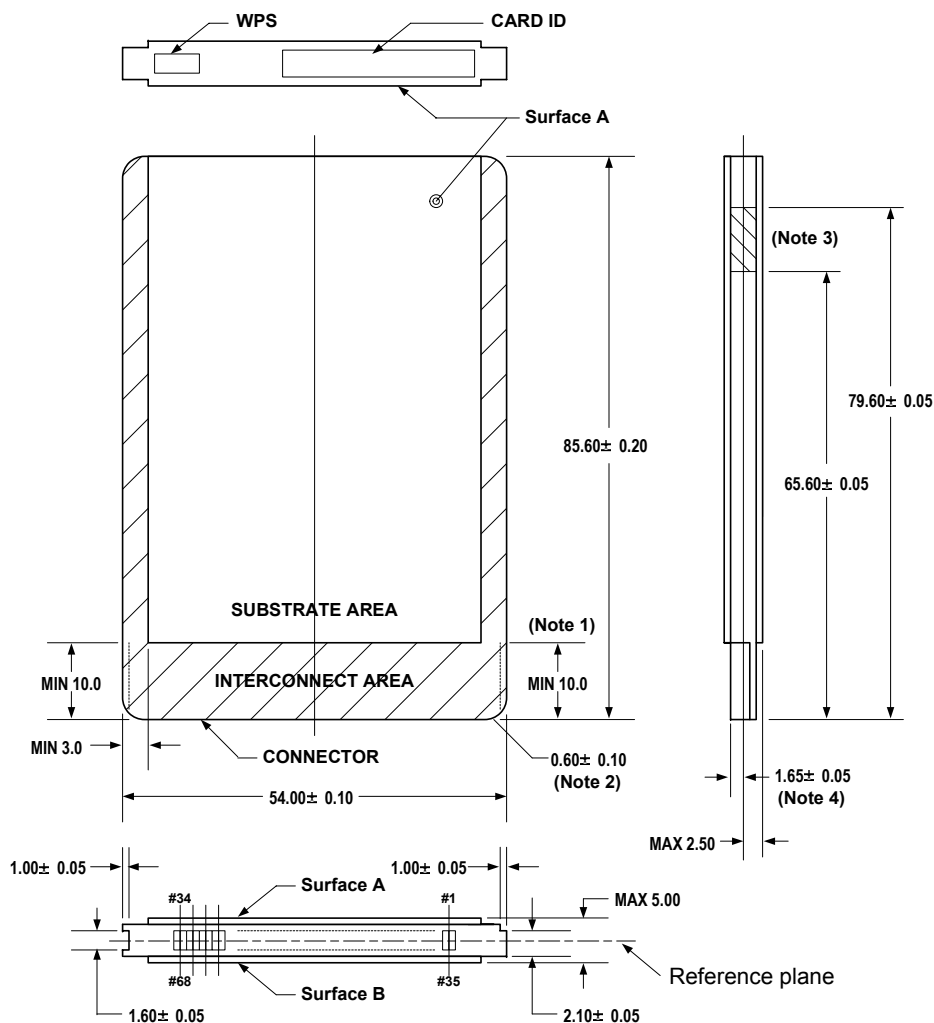
The mechanical and electrical performance of the Card connector shall be as specified in Table 5.1.

Table 5.1 – Mechanical and electrical performance

Item	Specification
Insertion Force	39.2 N maximum at speed of 25 mm/minute
Pulling Force	6.67 N minimum and 39.2 N maximum at speed of 25 mm/minute
Contact Resistance	Initially 40 mΩ maximum and 20 mΩ maximum change at voltage of 20 mV and current of 1 mA

5.4 Labeling

If a label is attached on surface A and/or surface B of a SSM Card, the thickness of the Card including the labels shall not exceed the thickness specified in Figure 5.1.



Dimensions in millimeters

- Note 1 - Polarization key length
 Note 2 - Dimension R corner radius
 Note 3 - Ground clip location
 Note 4 - Dimension is increased by 0.50 ± 0.05 mm over dimples

Figure 5.1 – SSM Card Package Dimensions

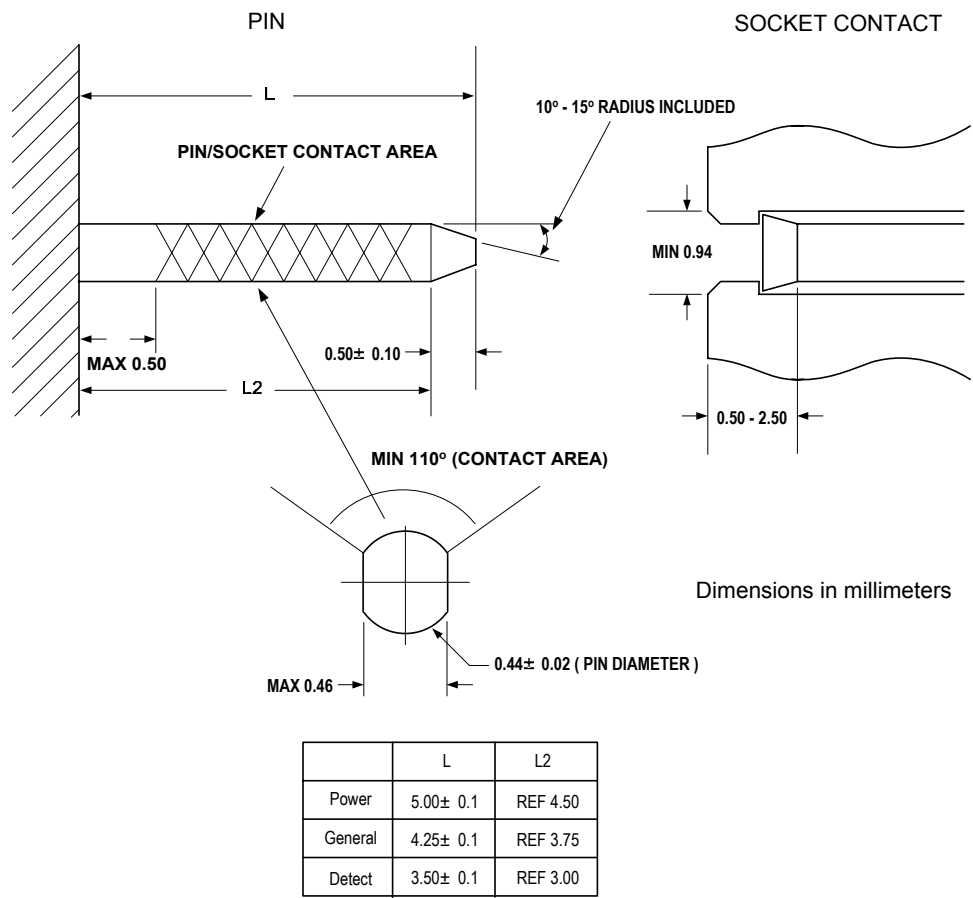


Figure 5.2 – SSM Card Socket Configuration

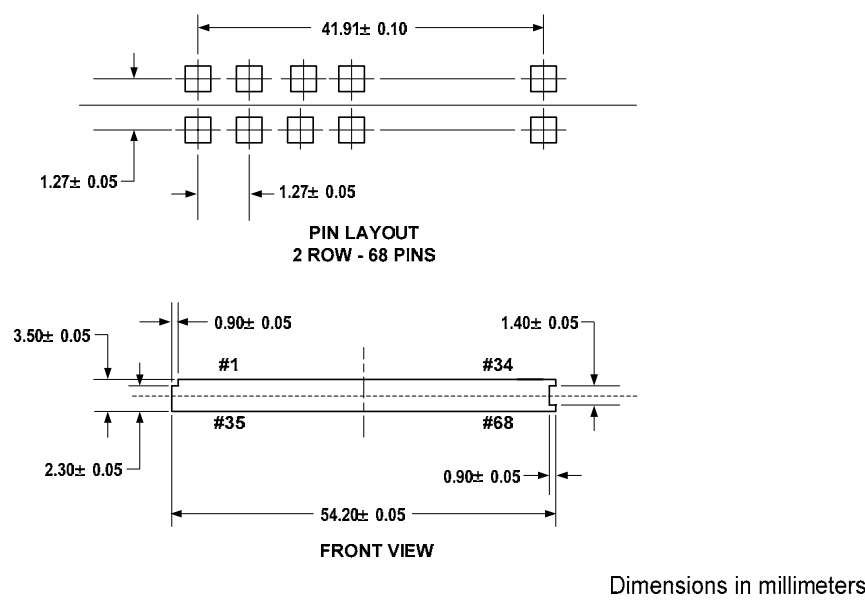


Figure 5.3 – SSM Card Pin Connector layout

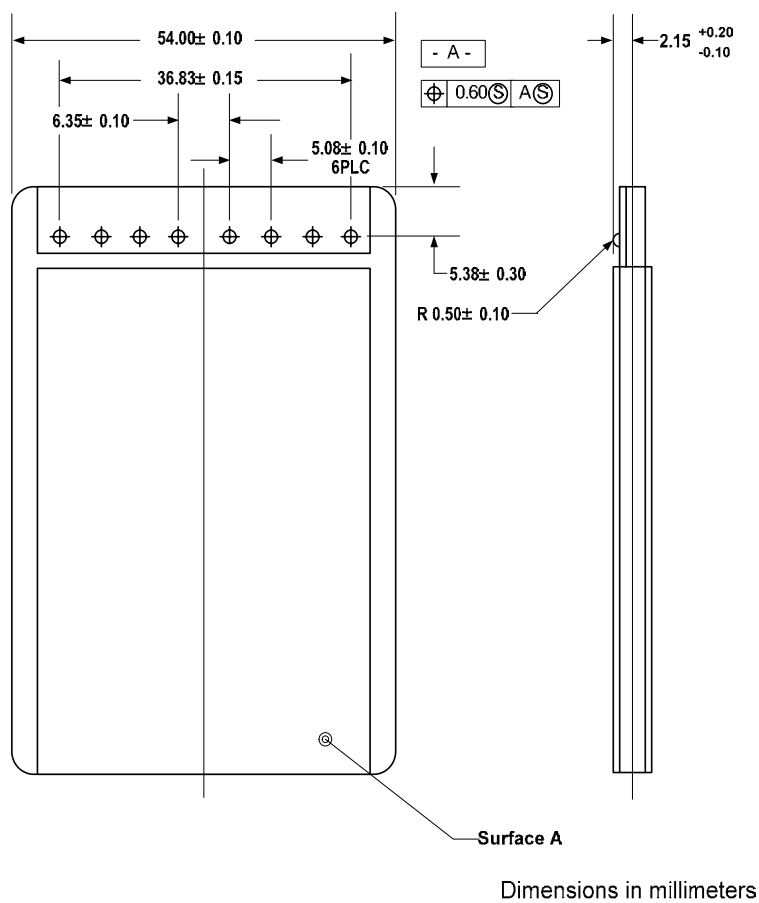


Figure 5.4 – SSM Card Pin Connector Dimensions

6 Electrical specification

6.1 Overview

This section defines the electrical specification of the SSM Card. The electrical interface of the SSM Card is a 32 bit high performance bus (SSM Card bus) with multiplexed address and data lines. The SSM Card bus specifies Card pin assignment and its signal definitions, Card detection mechanism, Electrical characteristics, Timing parameters and Bus operations.

NOTE – The bit order of the 32 bit bus shall follow the convention where bit 0 is LSB and bit 31 is MSB. Multi byte values are represented with little endian, the least significant byte first.

6.2 Signal Description

6.2.1 Pin assignment

The pin assignment of the SSM Card bus shall be as defined in Table 6.1.

Note: The name of the pins is the same as the PCI bus signal name when the first character "C" is deleted. The differences in the signals are summarized as follows:

- Card Detect pins and Voltage Sense pins are added.
- There is no IDSEL (Initialization Device Select) pin.
- There is only one interrupt pin (CINT#).
- A clock control signal (CCLKRUN#) is added.

Table 6.1 – SSM Card pin assignment

Pin	Signal	I/O	Signal type	Pin	Signal	I/O	Signal type
1	GND	DC		35	GND	DC	
2	CAD[0]	I/O	h/z	36	CCD1#	Output	
3	CAD[1]	I/O	h/z	37	CAD[2]	I/O	h/z
4	CAD[3]	I/O	h/z	38	CAD[4]	I/O	h/z
5	CAD[5]	I/O	h/z	39	CAD[6]	I/O	h/z
6	CAD[7]	I/O	h/z	40	Reserved		
7	CCBE[0]#	I/O	h/z	41	CAD[8]	I/O	h/z
8	CAD[9]	I/O	h/z	42	CAD[10]	I/O	h/z
9	CAD[11]	I/O	h/z	43	CVS[1]	I/O	
10	CAD[12]	I/O	h/z	44	CAD[13]	I/O	h/z
11	CAD[14]	I/O	h/z	45	CAD[15]	I/O	h/z
12	CCBE[1]#	I/O	h/z	46	CAD[16]	I/O	h/z
13	CPAR	I/O	h/z	47	Reserved		
14	CPERR#	I/O	s/h/z	48	Reserved		
15	CGNT#	Input		49	CSTOP#	I/O	s/h/z
16	CINT#	Output	o/d	50	CDEVSEL#	I/O	s/h/z
17	Vcc	DC in		51	Vcc	DC in	
18	Vpp	DC in		52	Vpp	DC in	
19	CCLK	Input		53	CTRDY#	I/O	s/h/z
20	CIRDY#	I/O	s/h/z	54	CFRAME#	I/O	s/h/z
21	CCBE[2]#	I/O	h/z	55	CAD[17]	I/O	h/z
22	CAD[18]	I/O	h/z	56	CAD[19]	I/O	h/z
23	CAD[20]	I/O	h/z	57	CVS[2]	I/O	
24	CAD[21]	I/O	h/z	58	CRST#	Input	
25	CAD[22]	I/O	h/z	59	CSERR#	Output	o/d
26	CAD[23]	I/O	h/z	60	CREQ#	Output	h/z
27	CAD[24]	I/O	h/z	61	CCBE[3]#	I/O	h/z
28	CAD[25]	I/O	h/z	62	Reserved		
29	CAD[26]	I/O	h/z	63	Reserved		
30	CAD[27]	I/O	h/z	64	CAD[28]	I/O	h/z
31	CAD[29]	I/O	h/z	65	CAD[30]	I/O	h/z
32	Reserved			66	CAD[31]	I/O	h/z
33	CCLKRUN#	I/O	o/d	67	CCD[2]#	Output	
34	GND	DC		68	GND	DC	

I/O: Input/Output, h/z: Tri-state, s/h/z :Sustained Tri-State, o/d : Open drain, # : Low active

NOTE – Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The detailed information is described in the PCI Local Bus Specification section 2.1.

6.2.2 Signal/Pin Description

6.2.2.1 Power and Ground pins

• Vcc

Vcc of the SSM Card shall be 3.3V ± 0.3V Voltage.

• Vpp

The voltage of the **Vpp** pin shall be the same voltage as the **Vcc** pin.

6.2.2.2 Interface Configuration pins

• CCD[2::1]#

CCD[2::1]# are the Card Detect pins that provide a means for sockets to detect the Card insertion and removal events. **CCD[2::1]#** pins are at opposite ends of the connector to ensure a valid insertion.

• CVS[2::1]#

CVS[2::1]# are in conjunction with **CCD[2::1]#** and used to encode card type information.

NOTE – See section 6.3 for details.

6.2.2.3 System pins

• CCLK

CCLK provides timing for all transactions on the SSM Card bus interface and is an input to every SSM Card bus device. All other SSM Card bus signals, except **CRST#** (upon assertion), **CCLKRUN#**, **CINT#**, **CCD[2::1]#**, and **CVS[2::1]**, are sampled on the rising edge of **CCLK**, and all timing parameters are defined with respect to this edge. The maximum frequency of **CCLK** shall be 33MHz. The clock may be stopped in the low state.

• CCLKRUN#

CCLKRUN# is a signal to control the clock and is used by Cards to request starting (or speeding up) the SSM Card bus clock, **CCLK**. **CCLKRUN#** also indicates the clock status. For SSM Cards, **CCLKRUN#** is an open drain output and also an input. For the host system, **CCLKRUN#** is a Sustained High-Z state I/O signal. The SSM Card does not support **CCLKRUN#**.

• CRST#

CRST# is used to bring SSM Card bus specific registers, sequencers, and signals to a consistent state. **CRST#** affects the reset states of required SSM Card configuration registers. Anytime **CRST#** is asserted, all SSM Card bus output signals shall be a High-Z state. **CSERR#**, **CINT#**, and **CCLKRUN#** (open drain) are floated. **CREQ#** shall be in a High-Z state (it cannot be driven low or high during reset). **CGNT#** must be negated. To prevent **CAD[31::00]**, **CCBE[3::0]#**, and **CPAR** signals from floating during reset, the central resource may drive these lines during reset but only to a low voltage level, they may not be driven high. **CVS[2::1]** shall be driven low. The states of **CCD[2::1]#** are not affected by **CRST#**. Negation of **CRST#** is synchronous to **CCLK**, but assertion of **CRST#** is not synchronous to **CCLK**.

NOTE – See section 6.2.3 for clock and signal timing details.

6.2.2.4 Address and Data pins

• CAD[31::00]

Address and Data are multiplexed in **CAD[31::00]** on the same SSM Card bus pins. A bus transaction shall consist of an address phase followed by one or more data phases. The SSM Card bus shall support both read and write bursts. The address phase is the clock cycle in which **CFRAME#** is asserted. During the address phase, **CAD[31::00]** contain a byte address for I/O and contain a 4 byte address for configuration and memory. During data phases, **CAD[07::00]** contain the least significant byte (LSB) and **CAD[31::24]** contain the most significant byte (MSB). Write data is stable and valid when **CIRDY#** is asserted. Read data is stable and valid when **CTRDY#** is asserted. Data is transferred during those clocks where both **CIRDY#** and **CTRDY#** are asserted.

• CCBE[3::0]#

Command and Byte Enables are multiplexed in **CCBE[3::0]#** on the same SSM Card bus pins. During the address phase of a transaction, **CCBE[3::0]#** define the bus command (see 6.4.2 for bus command definitions). During the data phase, **CCBE[3::0]#** are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. **CCBE[0]#** applies to **CAD[07::00]** (LSB) and **CCBE[3]#** applies to **CAD[31::24]** (MSB).

NOTE – See section 6.4.2 for details.

6.2.2.5 Interface Control Pins

• CFRAME#

CFRAME# is driven by the current master to indicate the beginning and duration of a transaction. **CFRAME#** is asserted to indicate that a bus transaction is beginning. While **CFRAME#** is asserted, data transfers continue. When **CFRAME#** is negated, the transaction is in the final data phase.

• CIRDY#

CIRDY# indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. **CIRDY#** is used in conjunction with **CTRDY#**. A data phase is completed on any clock both **CIRDY#** and **CTRDY#** are sampled asserted. During a write, **CIRDY#** indicates that valid data is present on **CAD[31::00]**. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both **CIRDY#** and **CTRDY#** are asserted together.

• CTRDY#

CTRDY# indicates the agent's (selected target's) ability to complete the current data phase of the transaction. **CTRDY#** is used in conjunction with **CIRDY#**. A data phase is completed on any clock both **CTRDY#** and **CIRDY#** are sampled asserted. During a read, **CTRDY#** indicates that valid data is present on **CAD[31::00]**. During a write, **CTRDY#** indicates the target is prepared to accept data. Wait cycles are inserted until both **CIRDY#** and **CTRDY#** are asserted together.

• CSTOP#

CSTOP# indicates the current target is requesting the master to stop the current transaction.

• CDEVSEL#

CDEVSEL#, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, **CDEVSEL#** indicates whether any device on the bus has been selected.

NOTE – The timing parameters are defined in section 6.4.2.1 and 6.4.2.2.

6.2.2.6 Arbitration Pins (Bus Masters Only)

• CREQ#

CREQ# indicates to the arbiter that this agent desires use of the bus. Every master has its own **CREQ#**.

• CGNT#

CGNT# indicates to the agent that access to the bus has been granted. Every master has its own **CGNT#**.

6.2.2.7 Error Reporting Pins

• CPAR

CPAR is even parity across **CAD[31::00]** and **CCBE[3::0]#**. Parity generation is required by all SSM Card bus agents. **CPAR** is stable and valid one clock after the address phase. For the data phases **CPAR** is stable and valid one clock after either **CIRDY#** is asserted on a write transaction or **CTRDY#** is asserted on a read transaction. Once **CPAR** is valid, it remains valid until one clock after the completion of the current data phase. (**CPAR** has the same timing as **CAD[31::00]** but delayed by one clock.) The master drives **CPAR** for address and write data phases; the target drives **CPAR** for read data phases.

• CPERR#

CPERR# is used for reporting of data parity errors during all SSM Card bus transactions. The **CPERR#** pin is sustained tri-state and shall be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of **CPERR#** is one clock for each data phase that a data parity error is detected. If sequential data phases each have a data parity error, the **CPERR#** signal asserts for more than a single clock. **CPERR#** shall be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a **CPERR#** until it has claimed the access by asserting **CDEVSEL#** and completed a data phase.

• CSERR#

CSERR# is used for reporting system errors where the result could be catastrophic. **CSERR#** is a pure open drain and is actively driven for a single SSM Card bus clock by the agent reporting the error. The assertion of **CSERR#** is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of **CSERR#** to the negated state is accomplished by a weak pull-up (same value as used for s/h/z) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore **CSERR#**. The agent that reports **CSERR#**s to the operating system does so anytime **CSERR#** is sampled asserted.

NOTE – See section 6.4.3 for details.

6.2.2.8 Interrupt Request Pin

• CINT#

CINT# is an optional signal which is defined as level sensitive, and asserted low (negative true), using an open drain output driver. The assertion and negation of **CINT#** is asynchronous to **CCLK**. The device driver may not make any assumptions about interrupt sharing. All SSM Card bus device drivers shall be able to share an interrupt (chaining) with any other logical device, including functions on the same multifunction card.

NOTE – See section 7.3.1 and 7.3.2 for details.