

for Television — Format for Transmission of DV Compressed Video, Audio and Data Over a Serial Data Transport Interface



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1 Scope

This standard specifies the data structure and the transmission format of DV compressed video, audio, and data over a serial data transport interface (SDTI [SMPTE 305.2M]). The standard is a combination of video, audio, subcode, and control data optimized for the connection between DV-compliant VCRs and disk systems. It ensures high-speed data stream transfer up to five times faster than real time. The video, audio, and subcode data comply with IEC 61834-2 for both 525/60 and 625/50 systems. The bit stream consists of 77-byte DIF data blocks, which are common to other DV based signals. The DIF blocks are mapped onto SDTI using a frame-bounded algorithm preserving ease of manipulating the video and audio data.

The layers of signal processing and related standards are shown in figure 1.

NOTE – For descriptions of the SDTI, refer to SMPTE 305.2M, and for descriptions of video, audio, and subcode data, refer to IEC 61834-2. The standard corresponds to data type [241_h] registered as DVCAM- 1 in SMPTE 305.2M.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

SMPTE 305.2M-2000, Television — Serial Data Transport Interface (SDTI)

IEC 61834-2 (1998-08), Recording — Helical-Scan Digital Video Cassette Recording System Using 6,35 mm Magnetic Tape for Consumer Use (525-60, 625-50, 1125-60 and 1250-50 Systems) — Part 2: SD Format for 525-60 and 625-50 Systems

3 SDTI header data

The SDTI header data shall contain the parameters specified in SMPTE 305.2M, and shall be repeated on every line. For information, the header data is shown in table 1, and the SDTI header data structure is as shown in figure 2.

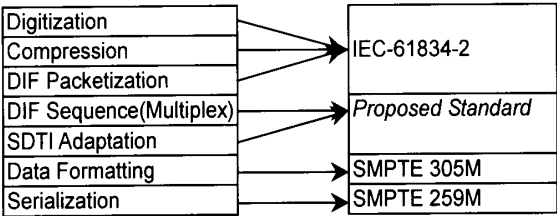


Figure 1 – Signal processing layers and related standards

Table 1 – Header data packet

Parameters	Length	Value
ADF	3 words	[000 _h] [3FF _h] [3FF _h]
DID	1 word	[140 _h]
SDID	1 word	[101 _h]
DC	1 word	[22E _h]
Line number	2 words	—
Line number CRC	2 words	—
Code	4 bits	[1 _h]
AAI	4 bits	—
Destination address	16 words	—
Source address	16 words	—
Block type	1 word	[1C1 _h]
CRC flag	1 word	[101 _h]
Reserved data	1 word	[200 _h]
Reserved data	4 words	[200 _h] [200 _h] [200 _h] [200 _h]
Header CRC	2 words	—
CS	1 word	—

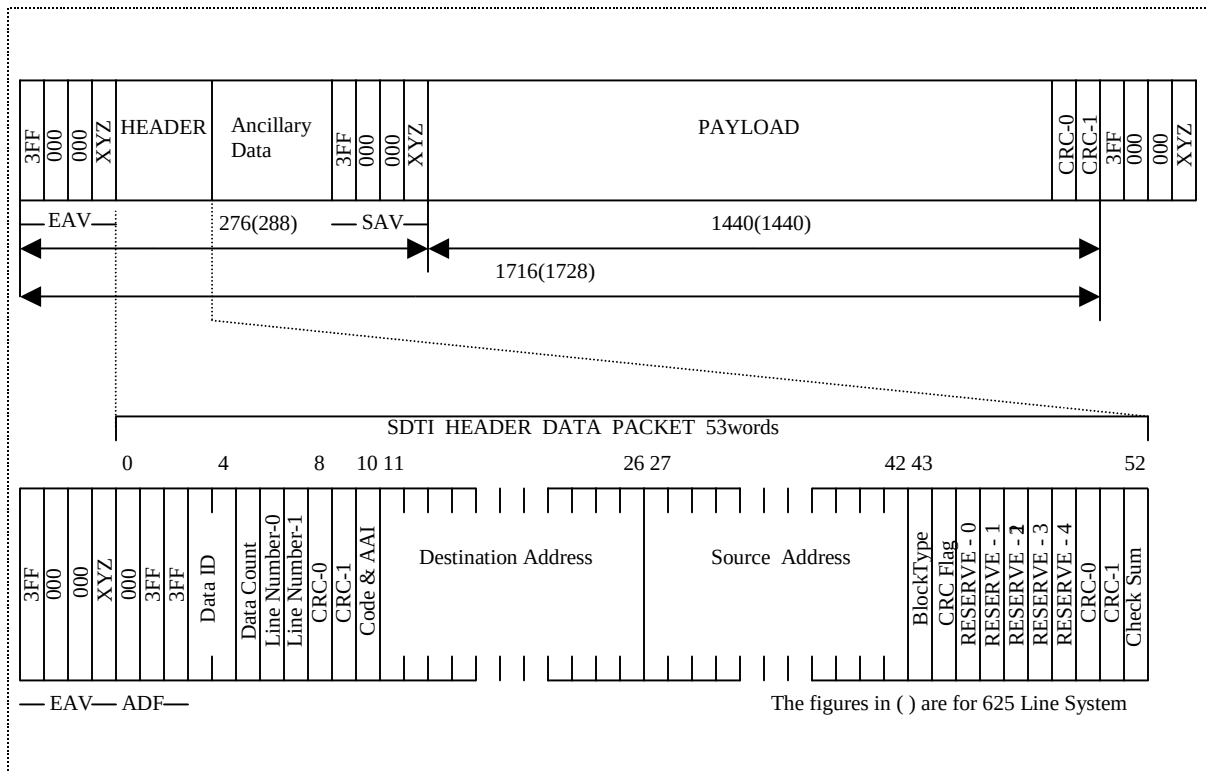


Figure 2 – SDTI header data structure

4 Data structure

The following clause describes the basic data structure and the system parameters of the bit stream. The data structure of the SDTI payload is shown in figure 3. The data block consists of a control data block and five vertical data slots, in which one compressed video stream shall be contained. The empty space and reserved area shall be set to 200_h as default value.

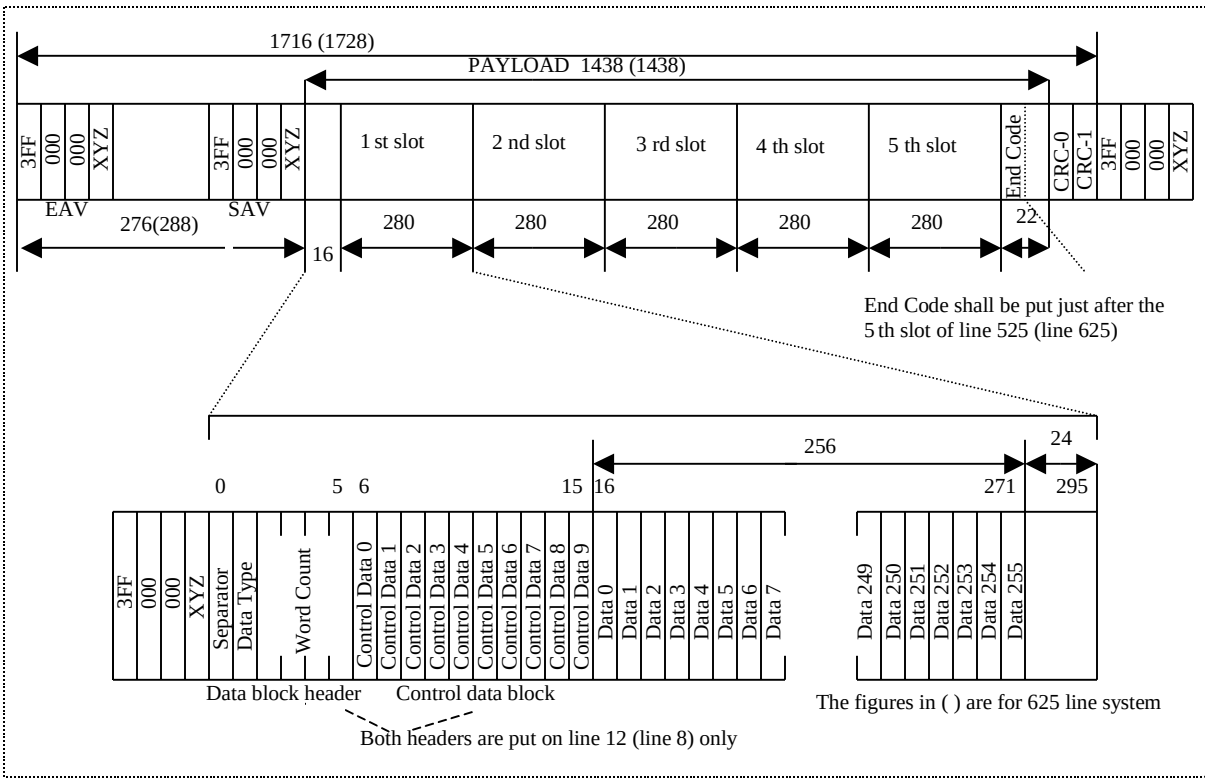


Figure 3 – Data structure

4.1 Data block

The control data block and the DIF data shall be contained in B0 (LSB) through B7 (8 bits). B8 shall be a reserved data bit for future expansion, which is normally set to zero. B9 shall be the complement of B8.

4.2 Data block header

The data block header, as specified in SMPTE 305.2M, shall contain the parameters shown in table 2. The data block header shall exist on line 12 for the 525/60 system or line 8 for the 625/50 system (refer to figures 7 and 10). The empty space for the Data block header and control data block on lines other than line 12 (line 8) shall be set to 200_h.

Table 2 – Data block header

Parameters	Length	Value
Separator	1 word	[309 _h]
Data type	1 word	[241 _h]
Word count	4 words	[B4720 _h] (525/60 system) [D8F50 _h] (625/50 system)

4.3 Control data block

A control data block shall be inserted immediately after the data block header. The control data block shall consist of 10 words (see figure 3), and the bits are allocated as shown in table 3. The control data block has some areas of commonality with the header section specified in IEC 61834-2, and also provides specific data required for data transfer between storage devices.

Byte 1: Indicates the data type (secondary).

Byte 2: Indicates the transfer conditions (transfer speed, locked/unlocked, audio and video validity).

Bytes 3-10: Common information to IEC 61834-2.

Table 3 – Control data block structure

MSB								LSB	
Byte 1	Secondary data type								
Byte 2	0 0 (RESERVE)		VIDEO INVALID	AUDIO INVALID	LOCK	TRANSFER MODE			
Byte 3	V 50/60	V STYPE	A 50/60	A STYPE	AP3	AP2	AP1	APT	
Byte 4	FF	FS	V REC MODE	BCSYS		DISP			
Byte 5	A-1 LF	A-1 CHN		A-1 PA	A-1 AUDIO MODE				
Byte 6	A-1 REC ST	A-1 REC END	A-1 REC MODE	A-1 EF	A-1 SMP			A-1 QU	
Byte 7	A-1 DRF	A-1 SPEED							
Byte 8	A-2 LF	A-2 CHN		A-2 PA	A-2 AUDIO MODE				
Byte 9	A-2 REC ST	A-2 REC END	A-2 REC MODE	A-2 EF	A-2 SMP			A-2 QU	
Byte 10	A-2 DRF	A-2 SPEED							
NOTES									
1 A-1 REC MODE: 1 when REC MODE of the AAUX source control pack is 111 (invalid recording); 0 when REC MODE of the AAUX source control pack is other than 111.									
2 A-2 REC MODE: 1 when REC MODE of the AAUX source control pack is 111 (invalid recording); 0 when REC MODE of the AAUX source control pack is other than 111.									
3 V REC MODE: 1 when REC MODE of the VAUX source control pack is 11 (invalid recording); 0 when REC MODE of the VAUX source control pack is other than 11.									
4 V STYPE, A STYPE, AP3, AP2, AP1, and APT are set to 0, which is the value for SD DV as specified in IEC 61834.									
5 A-1 QU and A-2 QU are 2-bit values and set to the values of QU (quantization) in the AAUX source packs specified in IEC 61834. Although IEC 61834 defines QU to have 3 bits, the actual specified values in IEC 61834 are within the 2 LSB bits, thus the 2 LSB bits can be used.									